



Hi-12F Specifications

Version V1.0

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Document development/revision/revocation resume

Vision	Data	Revised content	Edition	Approve
V1.0	2021.08.30	First Edition	Peihong Su	Ning Guan

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1. Product Overview

Hi-12F is a Wi-Fi module developed by Ai-Thinker. It can be widely used in intelligent terminal products related to the IoT, such as smart homes, smart security, and smart cities.

Hi-12F module is equipped with Hi3861V100 core processor chip. The chip is a highly integrated 2.4GHz low-power SoC WiFi chip that integrates IEEE 802.11b/g/n baseband and RF circuits. The RF circuit includes power amplifier PA, low noise amplifier LNA, RF balun, antenna switch and power supply Management and other modules. It supports 20MHz standard bandwidth and 5MHz/10MHz narrow bandwidth, and provides a maximum physical layer rate of 72.2Mbit/s. The WiFi baseband of the chip supports Orthogonal Frequency Division Multiplexing (OFDM) technology, and is backward compatible with Direct Sequence Spread Spectrum (DSSS) and Complementary Code Keying (CCK) technology, and supports various data in IEEE 802.11 b/g/n protocols rate.

The Hi3861V100 chip of the Hi-12F module also integrates a high-performance 32-bit microprocessor, a hardware security engine, and a wealth of peripheral interfaces. The peripheral interfaces include SPI, UART, I2C, PWM, GPIO, and multiple ADCs. It also supports high-speed SDIO2.0 Slave interface, the highest clock can reach 50MHz; The chip has built-in SRAM and Flash, which can run independently, and supports running programs on Flash.

The Hi-12F module supports Huawei LiteOS and third-party components, and provides an open and easy-to-use development and debugging environment.

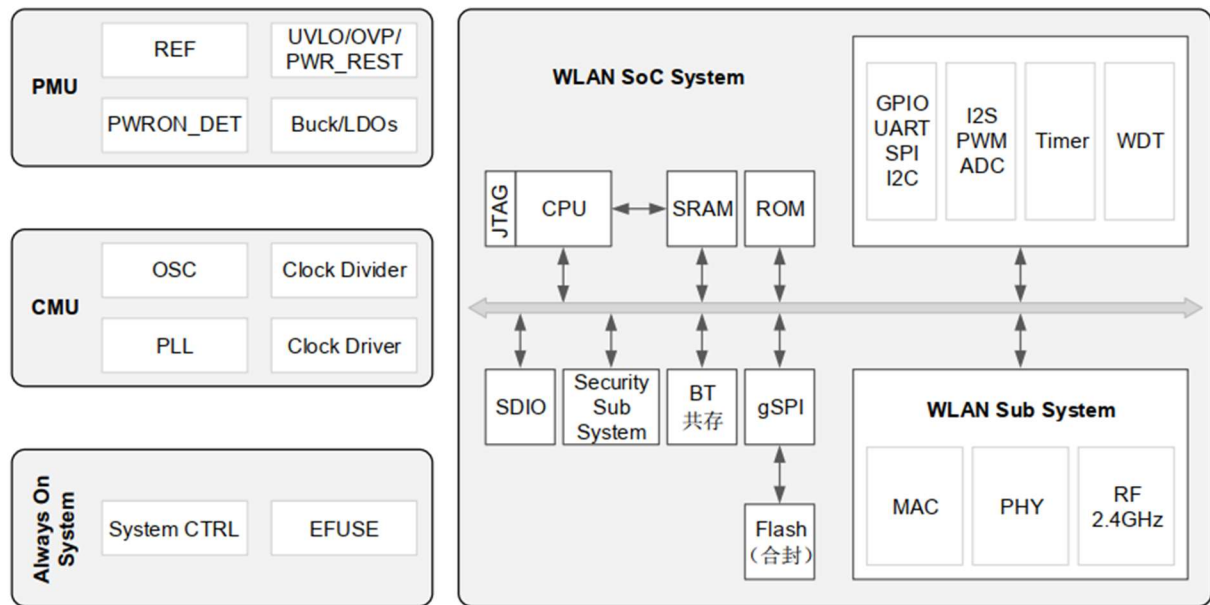


Figure 1 Main chip architecture diagram

1.1. Features

- 1×1 2.4GHz Frequency band (ch1~ch14)
- Support all data rates of IEEE802.11b/g/n single antenna
- Support maximum rate: 72.2Mbps@HT20 MCS7
- Support STBC
- Support Short-GI
- Support STA and AP form, as an AP, it supports up to 6 STAs to access.
- Support WPA WPA/WPA2 personal, WPS2.0
- High-performance 32bit microprocessor, with a maximum operating frequency of 160MHz.
- Embedded SRAM 352KB, ROM 288KB, embedded 2MB Flash
- Integrated EFUSE internally, supports secure storage, secure boot, and hardware ID
- Support 256 node Mesh networking
- Support AT command, can get started quickly
- Huawei LiteOS, an open operating system, provides an open, efficient and safe system development and operating environment
- Adopts SMD-22 package
- Support UART/SPI/I2C/GPIO/ADC/PWM/I2S/SDIO interface

2.Main parameters

Table 1 main parameter descriptions

Model Name	Hi-12F
Package	SMD-22
Size	24.0*16.0*3.2(±0.2)mm
Antenna	On-Board PCB
Frequency Range	2400 ~ 2483.5MHz
Operating Temperature	-40 °C ~ 85 °C
Store Temperature	-40 °C ~ 125 °C , < 90%RH
Power supply range	Voltage 3.0V ~ 3.6V, Electrical current >500mA
Support Interface	UART/SPI/I2C/GPIO/ADC/PWM /I2S/SDIO
UART Rate	Default 115200
WiFi	802.11b/g/n
Security	WFA WPA/WPA2 personal、WPS2.0

2.1. Electrical parameters

Hi-12F module is electrostatic sensitive devices and special precautions need to be taken when handling



Figure 2 ESD anti-static diagram

2.2. Electrical characteristics

Table 2 Main parameter description

Parameters		Conditions	Min	Typical values	Max	Unit
Supply voltage		VCC	3.0	3.3	3.6	V
I/O	Interface voltage	VDDIO1/ VDDIO2	3.125	3.3	3.6	V
	V _{IH}	-	2.4	-	3.63	V
	V _{IL}	-	-0.3	-	0.8	V
	V _{OH}	-	2.4	-	-	V
	V _{OL}	-	-	-	0.4	V

2.3. WIFI performance

Table 3 Description of main parameters

Description	Typical values	Unit
Operating frequency	2400 - 2483.5	MHz
Output power		
11n mode HT20, PA output power	14±2	dBm
11g mode, PA output power	15±2	dBm
11b mode, PA output power	17±2	dBm
Receiving sensitivity		
11b, 1 Mbps	≤-96	dBm
11b, 11 Mbps	≤-89	dBm
11g, 6 Mbps (1/2 BPSK)	≤-92	dBm
11g, 54 Mbps (3/4 64-QAM)	≤-74	dBm
11n, HT20 (MCS0)	≤-92	dBm
HT20 (MCS7)	≤-72	dBm

2.4. Power consumption

- The following power consumption data is measured based on a 3.3V power supply and an ambient temperature of 25°C.
- All measurements were completed at the antenna interface without SAW filters
- All emission data are based on 50% duty cycle, measured in continuous emission mode.

Table 4 Description of main parameters

Mode	Mix	Typical values	Max	Unit
Tx 802.11b, CCK 11Mbps, POUT=+17dBm	-	275	-	mA
Tx 802.11g, OFDM 54Mbps, POUT =+15dBm	-	255	-	mA
Tx 802.11n, MCS7, POUT =+14dBm	-	235	-	mA
Rx 802.11b, 1024 bit	-	50	-	mA
Rx 802.11g, 1024 bit	-	50	-	mA
Rx 802.11n, 1024 bit	-	50	-	mA
Ultra Deep Sleep	-	4	-	μA
DTIM1	-	715	-	μA
DTIM3	-	485	-	μA
DTIM10	-	310	-	μA

3.Appearance dimensions

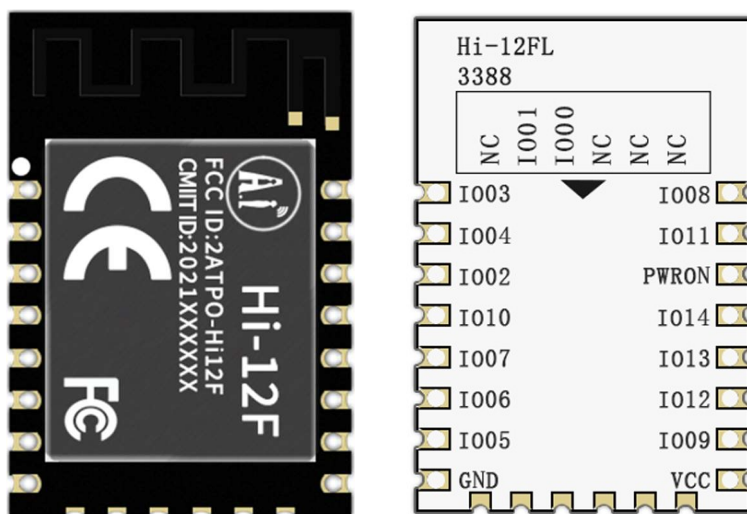


Figure 3 The appearance of the module(For reference only)

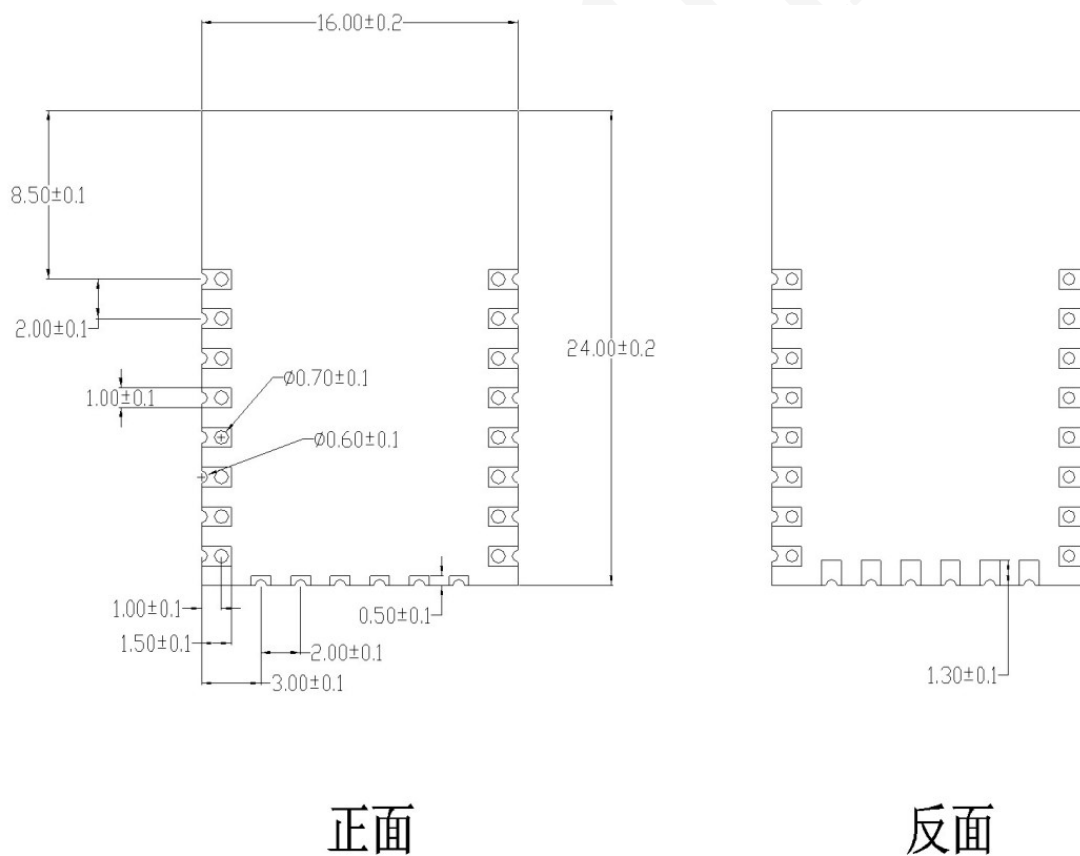


Figure 4 Module size diagram

4.Pin definition

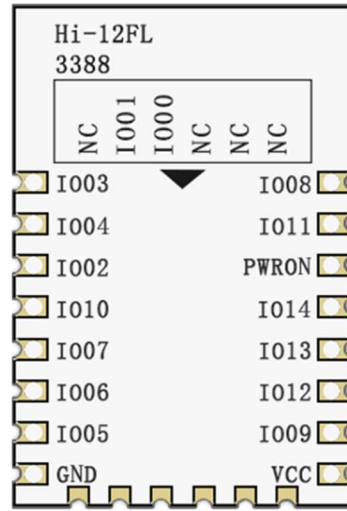


Figure 5 Schematic diagram of the pin

The Hi-12F series modules have 22 interfaces. As shown in the pin diagram, the pin function definition table is the interface definition.

Table 5 Hi-07F Pin function definition

No.	Name	Function
1	IO08	GPIO_08,UART1_RTS,SPI0_TXD,PWM1_OUT,I2S0_WS,WLAN_ACTIVE,JTAG_ENABLE
2	IO11	GPIO_11, UART2_TXD, SPI0_RXD, SDIO_CMD, ADC5, PWM2_OUT, I2S0_RX, HW_ID6
3	PWRON	Chip PMU power-on enable pin, pulled up inside the module 0: Power off 1: Power on
4	IO14	GPIO_14, UART0_LOG_RXD, UART2_CTS, SDIO_D1, PWM5_OUT, I2C0_SCL, HW_ID2
5	IO13	GPIO_13,UART0_LOG_TXD,UART2_RTS,SDIO_D0,ADC6,PWM4_OUT, I2S0_WS, I2C0_SDA
6	IO12	GPIO_12, UART2_RXD, SPI0_CS1, SDIO_CLK, ADC0, PWM3_OUT, I2S0_CLK, HW_ID7
7	IO09	GPIO_09, UART2_RTS, SPI0_TXD, SDIO_D2, ADC4, PWM0_OUT, I2S0_MCK, I2C0_SCL
8	VCC	Power supply, recommended 3.3V, > 500mA

9	NC	NC
10	NC	NC
11	NC	NC
12	IO00	GPIO_00, UART1_TXD, SPI1_CLK, PWM3_OUT, I2C1_SDA, JTAG_TDO, HW_ID0
13	IO01	GPIO_01, GPIO_01, UART1_RXD, SPI1_RXD, PWM4_OUT, I2C1_SCL, BT_FREQ, JTAG_TCK, HW_ID1
14	NC	
15	GND	Grounded
16	IO05	GPIO_05, UART1_RXD, SPI0_CS1, ADC2, PWM2_OUT, I2S0_MCK, BT_STATUS, HW_ID4
17	IO06	GPIO_06, UART1_TXD, SPI0_CLK, PWM3_OUT, I2S0_TX, COEX_SWITCH, JTAG_MODE
18	IO07	GPIO_07, UART1_CTS, SPI0_RXD, ADC3, PWM0_OUT, I2S0_CLK, BT_ACTIVE, HW_ID5
19	IO10	GPIO_10, UART2_CTS, SPI0_CLK, SDIO_D3, PWM1_OUT, I2S0_TX, I2C0_SDA
20	IO02	GPIO_02, UART1_RTS, SPI1_TXD, PWM2_OUT, JTAG_TRSTN, REFCLK_FREQ_STATUS
21	IO04	GPIO_04, UART0_LOG_RXD, ADC1, PWM1_OUT, I2C1_SCL, JTAG_TMS, HW_ID3
22	IO03	GPIO_03, UART0_LOG_TXD, UART1_CTS, SPI1_CS1, PWM5_OUT, I2C1_SDA, JTAG_TDI

Table 6 Module start mode description

System start up mode			
Pin	Default state	Low level	High level
IO2/REFCLK_FREQ_STATUS	Pull down	40MHz (Default)	24MHz
IO6/JTAG_MODE	Pull down	Normal function mode (Default)	DFT Test mode
IO8/JTAG_ENABLE	Pull down	Ordinary IO (Default)	JTAG enable

Note: IO2/IO6/IO8 are hardware configuration words, which cannot be in high level state when power on, otherwise the module cannot enter normal working state.

5. Schematic diagrams

5.1. Schematic diagrams of module

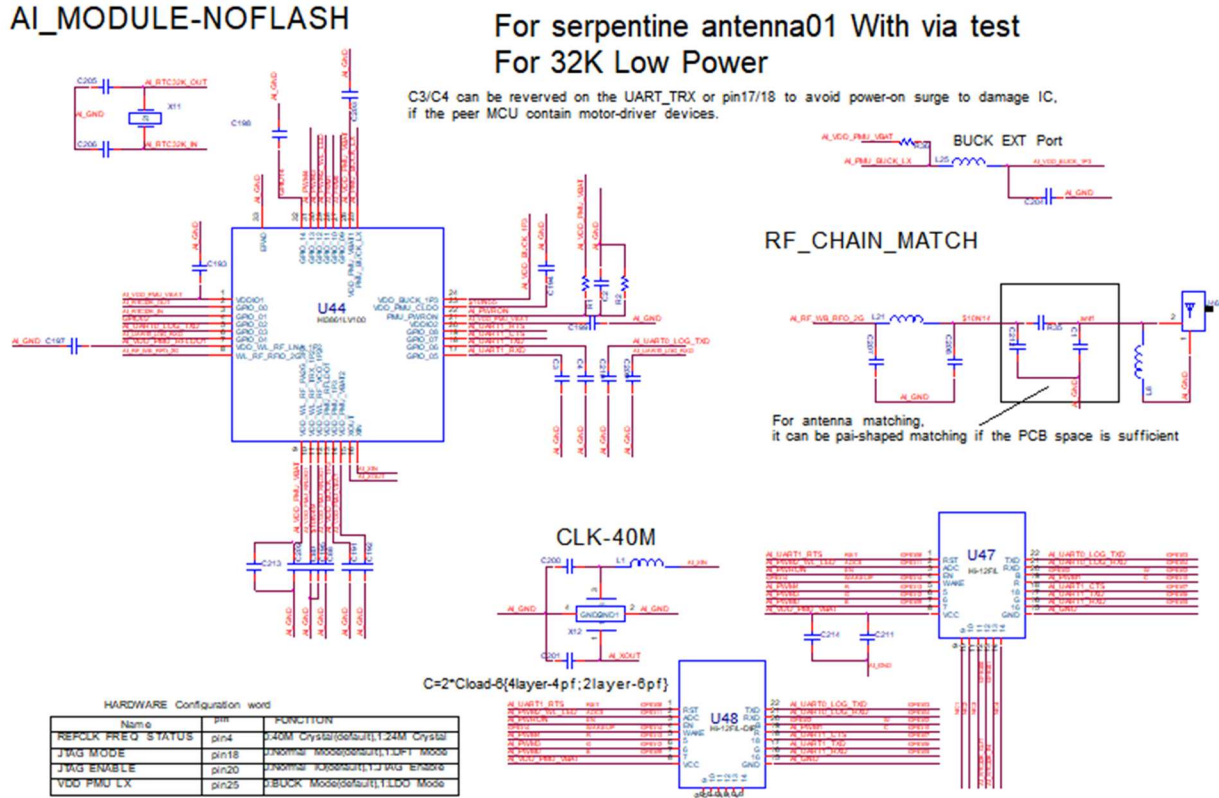


Figure 6 Module schematic diagram

Figure 7 Application circuit diagram

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6.Design guidance

6.1. Antenna layout requirements

(1) The installation position on the motherboard, the following two ways are recommended:
Solution 1: Put the module on the edge of the main board, and the antenna area extends out of the edge of the main board.

Solution 2: Put the module on the edge of the motherboard, and hollow out an area at the antenna position on the edge of the motherboard

(2) In order to meet the performance of the on-board antenna, it is forbidden to place metal parts around the antenna, away from high-frequency components.

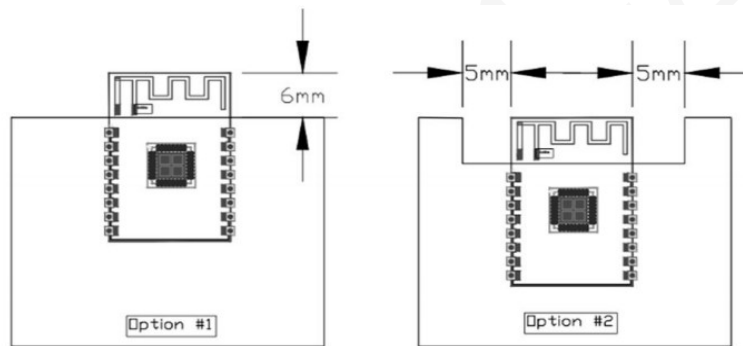


Figure 8 Schematic diagram of antenna layout

6.2. Power Supply

- (1) Recommended 3.3V voltage, peak current above 500mA
- (2) It is recommended to use LDO power supply; if using DC-DC, it is recommended that the ripple be controlled within 30mV.
- (3) It is recommended to reserve the position of the dynamic response capacitor for the DC-DC power supply circuit, which can optimize the output ripple when the load changes greatly.
- (4) 3.3V power interface recommends adding ESD devices

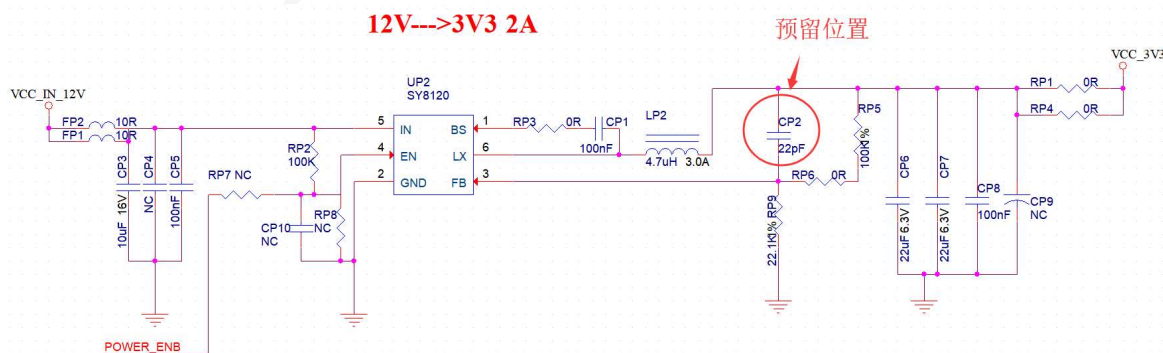


Figure 9 DC-DC step-down circuit diagram

6.3. GPIO

- (1) There are some GPIO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This can suppress overshoot and make the levels on both sides more stable. Helps both EMI and ESD
- (2) For the pull-up and pull-down of special IO ports, please refer to the instructions in the specification. This will affect the startup configuration of the module.
- (3) The IO port of the module is 3.3V. If the main control and the IO level of the module do not match, a level conversion circuit needs to be added.
- (4) If the IO port is directly connected to a peripheral interface, or a terminal such as a header, it is recommended to reserve an ESD device near the terminal of the IO trace

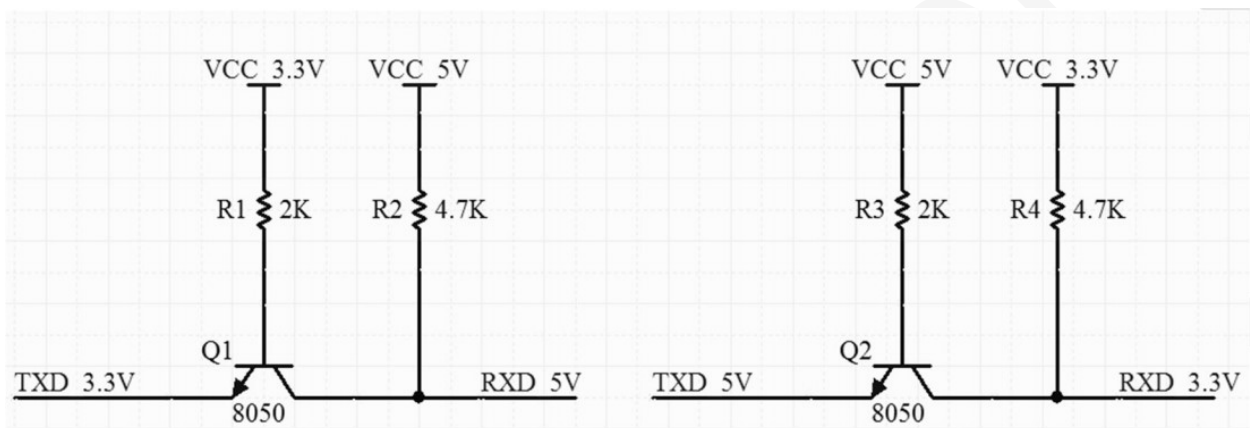


Figure 10 Level conversion circuit

7. Reflow soldering

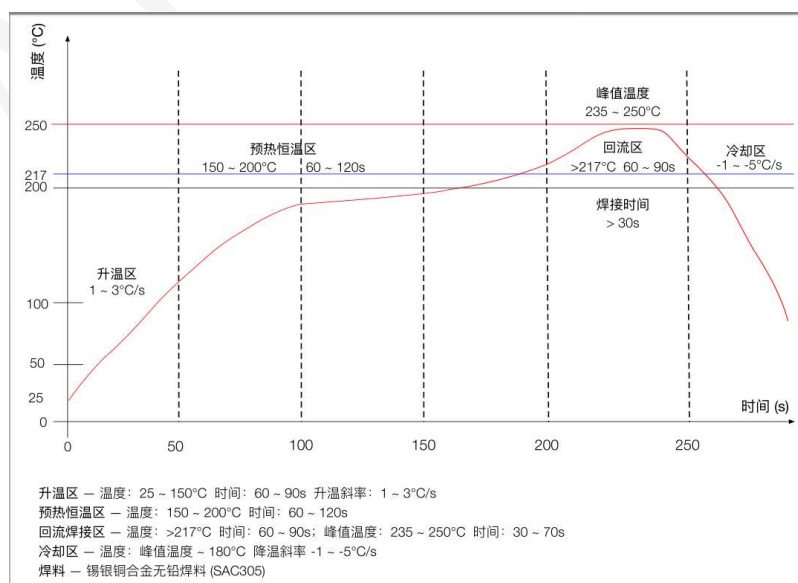


Figure 11 Reflow soldering

8. Packaging information

As shown in the figure below, Hi-12F is packed with tape



Figure 12 Schematic diagram of packaging

9. Product related model

Table 7 Table of related models

Model	Chip	Package	Size	Antenna
Hi-12F	Hi3861V100	SMD-22	24.0*16.0*3.2(± 0.2)mm	On-board
Hi-12FL	Hi3861LV100	SMD-22	24.0*16.0*3.2(± 0.2)mm	On-board
Hi-07S	Hi3861V100	SMD-22	17.0*16.0*3.2(± 0.2)mm	IPEX
Hi-07SL	Hi3861LV100	SMD-22	17.0*16.0*3.2(± 0.2)mm	IPEX
Product related information: https://docs.ai-thinker.com				

10. Contact us

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