ESP-12H Specification

Version V1.0

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Document Development/Revision/Repeal Resume

Version	Date	Developed/revised content	Make	Verify
V1.0	2020.09.23	First developed	Chaomei Deng	

CONTENT

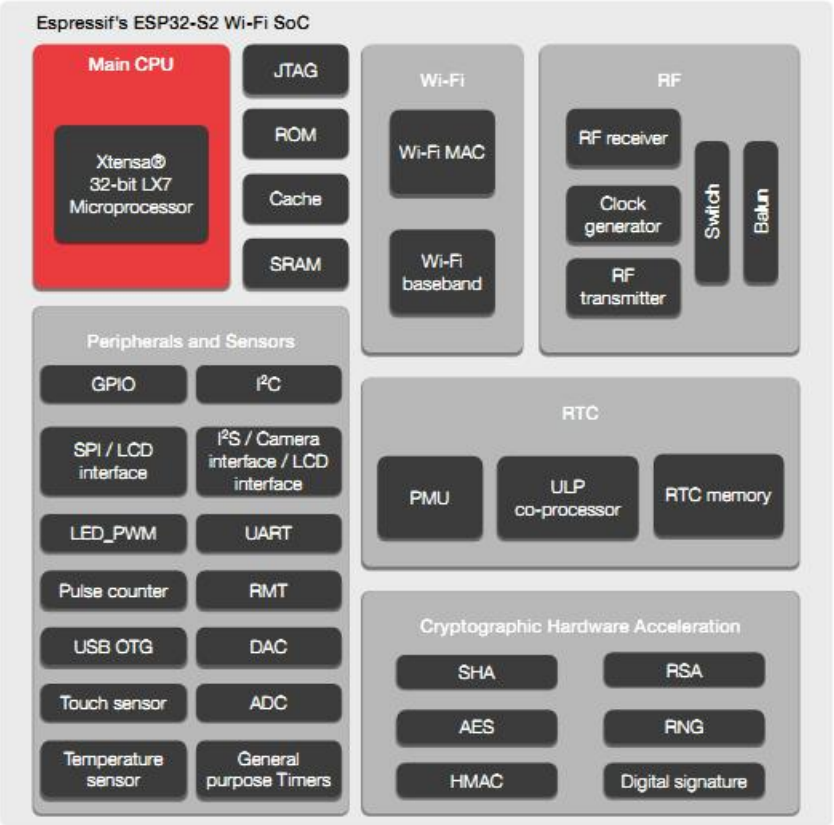
1. Product description

ESP-12H is a Wi-Fi module developed by Shenzhen Anxinke Technology Co., Ltd. The core processor of the module ESP32-S2F is a highly integrated low-power Wi-Fi system-on-chip (SoC), designed for Designed for various applications such as Internet of Things (IoT), mobile devices, wearable electronic devices, and smart homes. ESP32-S2F has industry-leading low-power performance and RF performance, supports IEEE802.11b/g/n protocol, integrates Wi-Fi MAC, Wi-Fi RF and baseband, RF switch, RF Balun, power amplifier, low noise Amplifier etc.

The ESP32-S2F chip is equipped with an Xtensa® 32-bit LX7 single-core processor with a working frequency of up to 240 MHz. The chip supports secondary development without using other microcontrollers or processors. The chip has built-in 2 MB SRAM and 128 KB ROM. ESP32-S2F supports a variety of low-power consumption working states, which can meet the power consumption requirements of various application scenarios. The chip's unique features such as fine clock gating function, dynamic voltage clock frequency adjustment function, and RF output power adjustable function can achieve the best balance between communication distance, communication rate and power consumption.

ESP32-S2F provides a wealth of peripheral interfaces, including SPI, I2S, UART, I2C, LED PWM interface, ADC, touch sensor, temperature sensor and up to 22 GPIOs. It also includes a full-speed USB On-The-Go (OTG) interface that can support the use of USB communication.

ESP32-S2F has a variety of unique hardware security mechanisms. The hardware encryption accelerator supports AES, SHA and RSA algorithms. Among them, RNG, HMAC and digital signature (Digital Signature) modules provide more security features. Other security features include flash encryption and secure boot (se-cure boot) signature verification. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.



1.2 Characteristics

- Complete 802.11b/g/n Wi-Fi SoC module, data rate up to 150Mbps
- Built-in ESP32-S2F chip, Xtensa® single-core 32-bit LX7 microprocessor, supporting clock frequency up to 240 MHz, with 128KB ROM, 320KB SRAM, 16KB RTC SRAM
- Support UART/GPIO/ADC/PWM/I2C/I2S/USB interface, support touch sensor, temperature sensor, pulse counter
- Using SMD-22 package
- Intergrate Wi-Fi MAC/ BB/RF/PA/LNA
- Support multiple sleep modes, deep sleep current is less than 10uA

- Serial port rate up to 4Mbps
- Built-in Lwip protocol stack
- Support STA/AP/STA+AP working mode
- Support Smart Config (APP)/AirKiss (WeChat) for Android and IOS, one-click network configuration
- Support serial port local upgrade and remote firmware upgrade (FOTA)
- General AT commands can be used quickly
- Support secondary development, integrated Windows and Linux development environment
- About Flash

  ESP-12H chip has built-in 2MByte Flash.

1.1 Main parameter

List 1 Main parameter description

Model	ESP-12H
Package	SMD-22
Size	24.0*16.0*3.0(±0.2)MM
Antenna	PCB antenna/IPEX port
Spectrum range	2400 ~ 2483.5MHz
Work temperature	-40 ℃ ~ 85 ℃
Storage environment	-40 ℃ ~ 125 ℃ , < 90%RH
Power supply	Voltage 3.0V ~ 3.6V， Current >500mA
Interface	UART/GPIO/ADC/PWM/I2C/I2S
IO ports	IO0,IO1,IO2,IO4,IO5,IO7,IO8,IO9,IO10,IO11,IO12,IO19,IO20 , IO21,IO33,IO34,IO37,IO38
Serial port rate	Support 110 ~ 4608000 bps ， Default 115200 bps

Safety	WEP/WPA-PSK/WPA2-PSK
SPI Flash	Built-in 2MByte

2. Electrical parameters

2.1 Electrical characteristics

Parameter		Condition	Min	Typical	Max	Unit
Voltage		VDD	3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}	-	-0.3/0.75VIO	-	0.25VIO/3.6	V
	V_{OL}/V_{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I_{MAX}	-	-	-	12	mA

2.2 RF performance

Description	Typical	Unit
Work frequency	2400 - 2483.5	MHz
Output power		
11n mode HT40, PA output power is	13±2	dBm
11n mode HT20, PA output power is	13±2	dBm
In 11g mode, the PA output power is	15±2	dBm
In 11b mode, the PA output power is	18±2	dBm
Receiving sensitivity		
CCK, 1 Mbps	<=-97	dBm
CCK, 11 Mbps	<=-88	dBm
6 Mbps (1/2 BPSK)	<=-92	dBm

54 Mbps (3/4 64-QAM)	<=-75	dBm
HT20 (MCS7)	<=-72	dBm
HT40 (MCS7)	<=-69	dBm

2.3 Power consumption

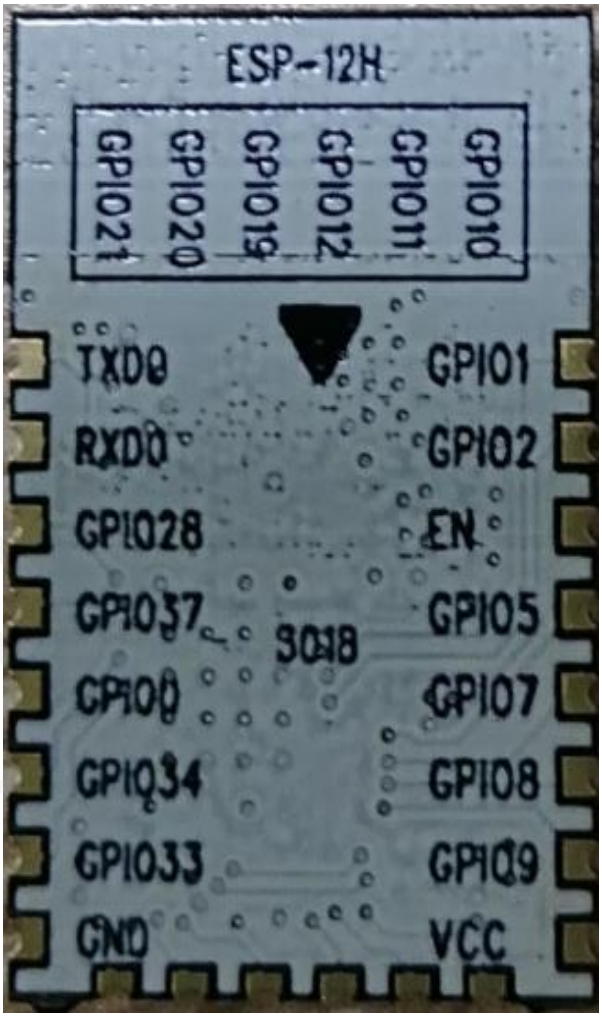
The following power consumption data is based on a 3.3V power supply, an ambient temperature of 25°C, and measured using an internal voltage regulator.

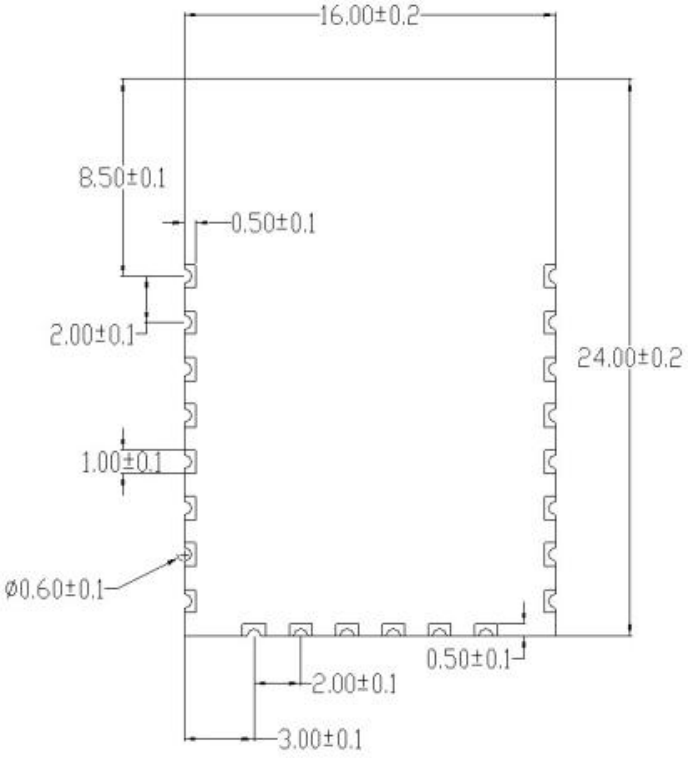
- All measurements are done at the antenna interface without SAW filter.
- All emission data is based on 90% duty cycle, measured in continuous emission mode.

Mode	Mix	Typical	Max	Unit
Transmit 802.11b, CCK 1Mbps, POUT=+19.5dBm	-	190	-	mA
Transmit 802.11g, OFDM 54Mbps, POUT =+15dBm	-	145	-	mA
Transmit 802.11n, MCS7, POUT =+13dBm	-	135	-	mA
Receive 802.11b, packet length 1024 bytes, -80dBm	-	63	-	mA
Receive 802.11g, packet length 1024 bytes, -70dBm	-	63	-	mA
Receive 802.11n, packet length 1024 bytes, -65dBm	-	68	-	mA
Modem-Sleep①	-	19	-	mA
Light-Sleep②	-	450	-	μA
Deep-Sleep③	-	235	-	μA
Power Off	-	1	-	μA

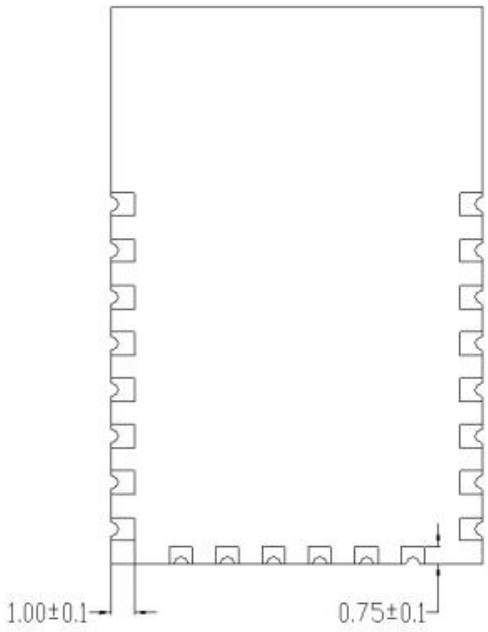
3. Physical dimension

3.1 ESP-12H appearance



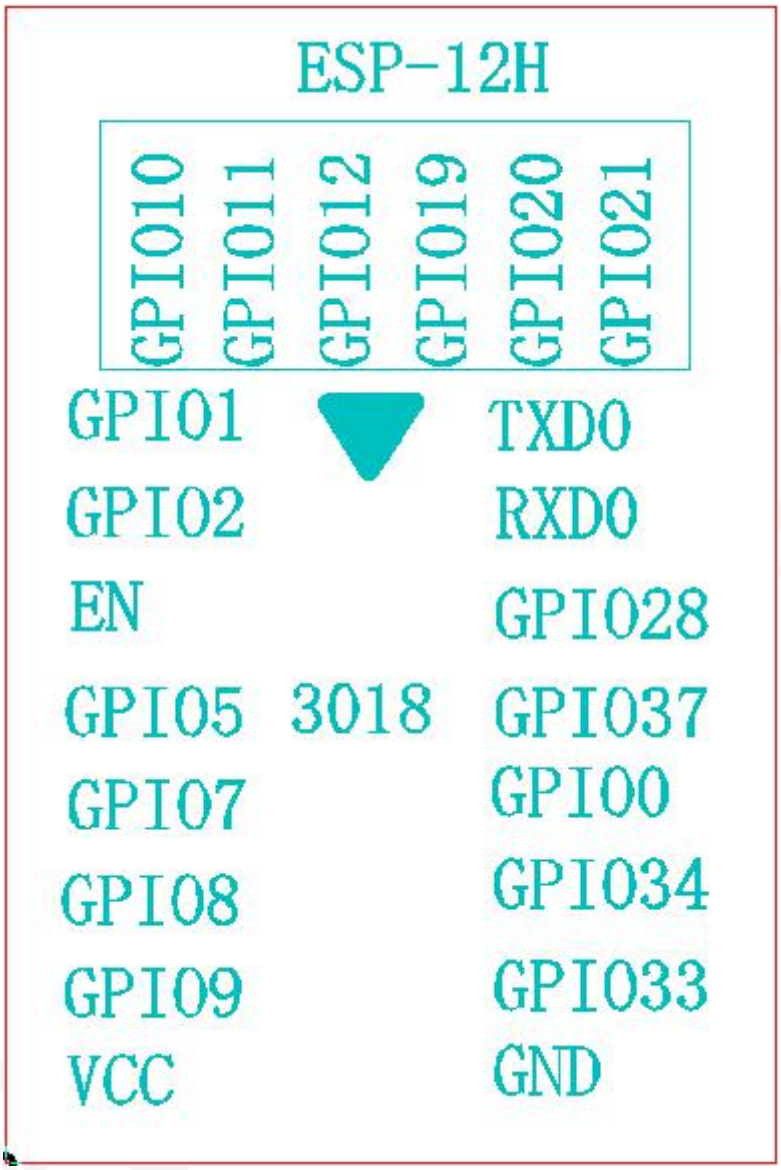


正面



背面

4. Pin definition



The ESP-12H module has a total of 22 interfaces, as shown in the pin diagram, the pin function definition table is the interface definition.

ESP-12H Pin diagram

List PIN function definition

Item No.	Name	Function description
1	U0TX	U0TX,GPIO43,CLK_OUT1
2	U0RX	U0RX,GPIO44,CLK_OUT2
3	IO28	SPIWP,GPIO28
4	IO37	SPIDQS, GPIO37,FSPIQ

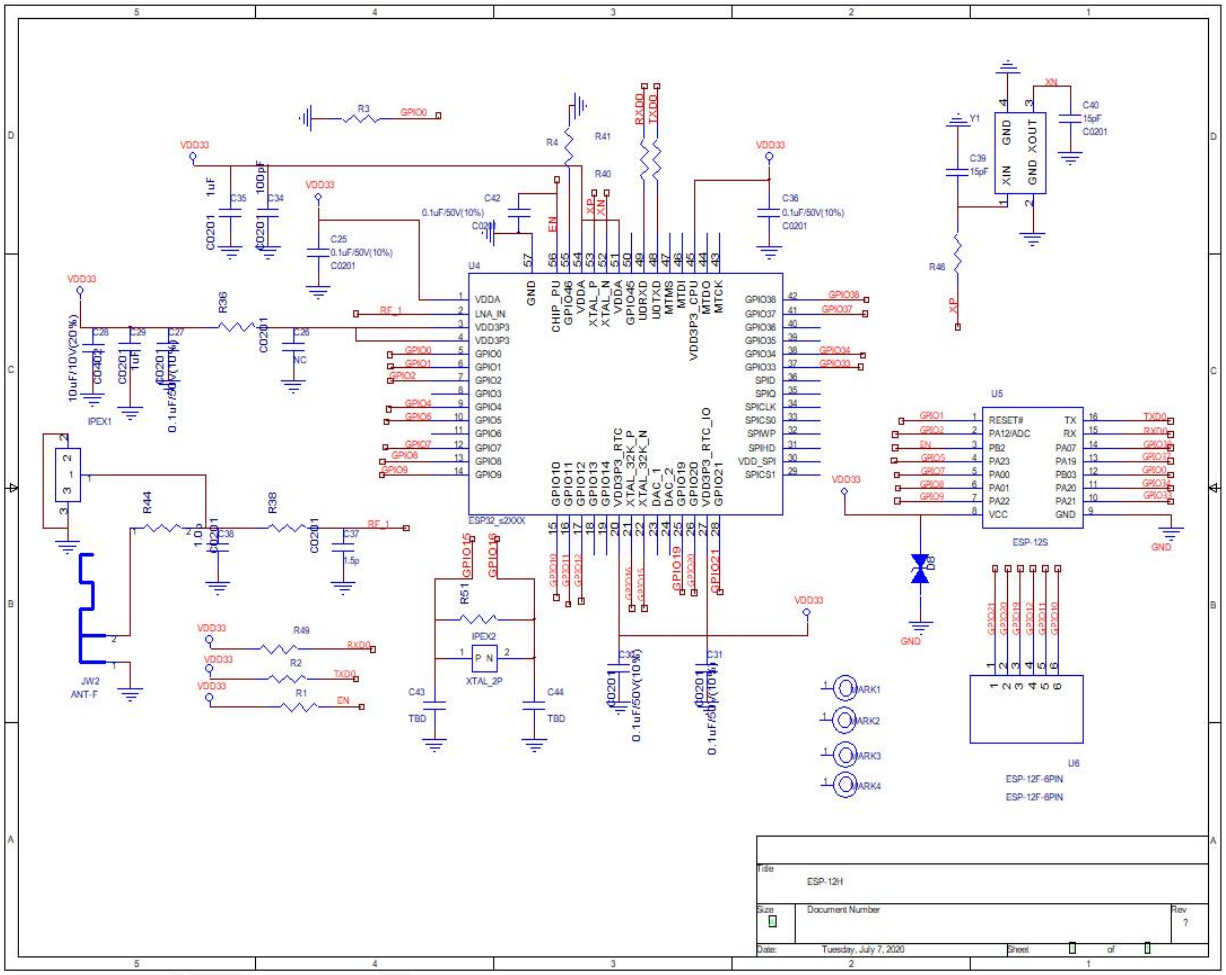
5	IO0	RTC_GPIO0, GPIO0
6	IO34	SPIIO5,GPIO34,FSPICSO
7	IO33	SPIIO4,GPIO33,FSPIHD
8	GND	GND
9	IO21	RTC_GPIO21, GPIO21
10	IO20	RTC_GPIO20,GPIO20,U1CTS,ADC2_CH9,CLK_OUT1,USB_D+
11	IO19	RTC_GPIO19,GPIO19,U1RTS,ADC2_CH8,CLK_OUT2,USB_D-
12	IO12	RTC_GPIO12,GPIO12,TOUCH12,ADC2_CH1,FSPICLK,FSPIIO6
13	IO11	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPID,FSPIIO5
14	IO10	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPICS0, FSPIIO4
15	VCC	VCC
16	IO9	RTC_GPIO9,GPIO9,TOUCH9,ADC1_CH8,FSPIHD
17	IO8	RTC_GPIO8,GPIO8,TOUCH8,ADC1_CH7
18	IO7	RTC_GPIO7,GPIO7,TOUCH7,ADC1_CH6
19	IO5	RTC_GPIO5,GPIO5,TOUCH5,ADC1_CH4
20	EN	High level: chip enable; Low level: the chip is turned off; Be careful not to leave the CHIP_PU pin floating;
21	IO2	RTC_GPIO2,GPIO2,TOUCH2,ADC1_CH1
22	IO1	RTC_GPIO1,GPIO1,TOUCH1,ADC1_CH0

List Module startup mode description

System startup mode			
PIN	Default	SPI boot mode	Download start mode
IO0	Pull up	1	0
IO46	Pull down	Irrelevant	0

Note: Some pins have been internally pulled up, please refer to the schematic

5. Schematic diagram



6. Design guide

1.note:

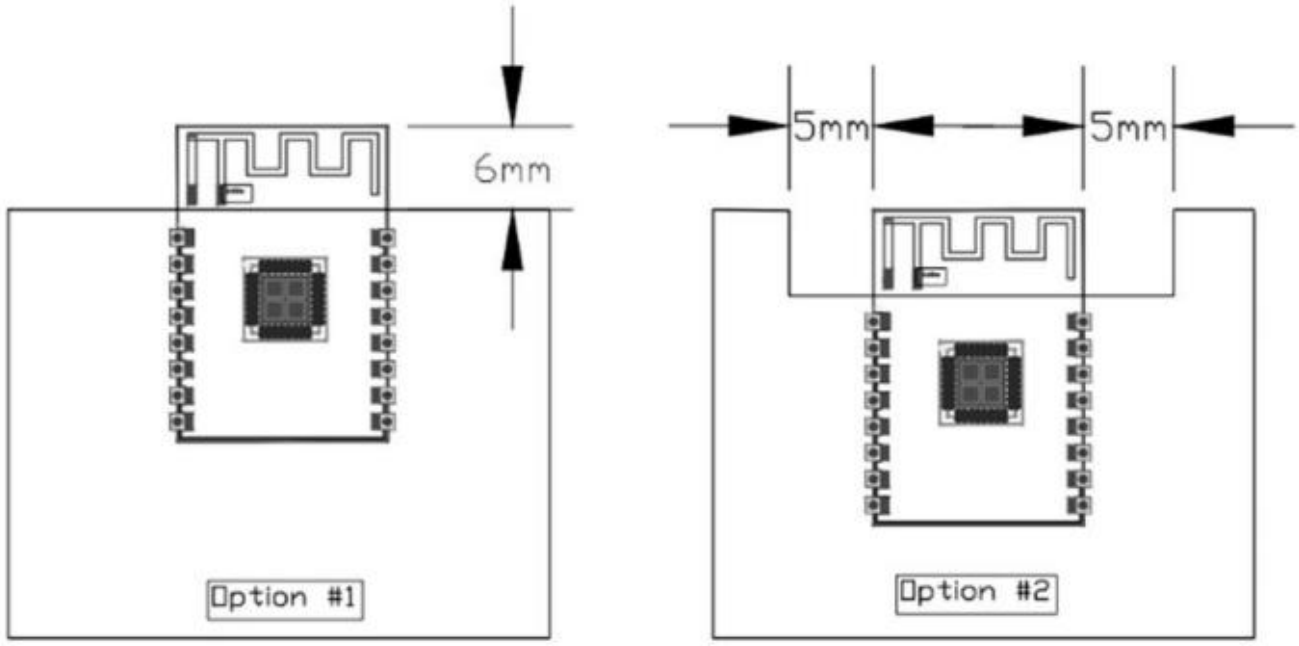
(1) The EN pin needs to add an RC delay circuit, it is recommended that R=10kΩ, C=0.1μF;

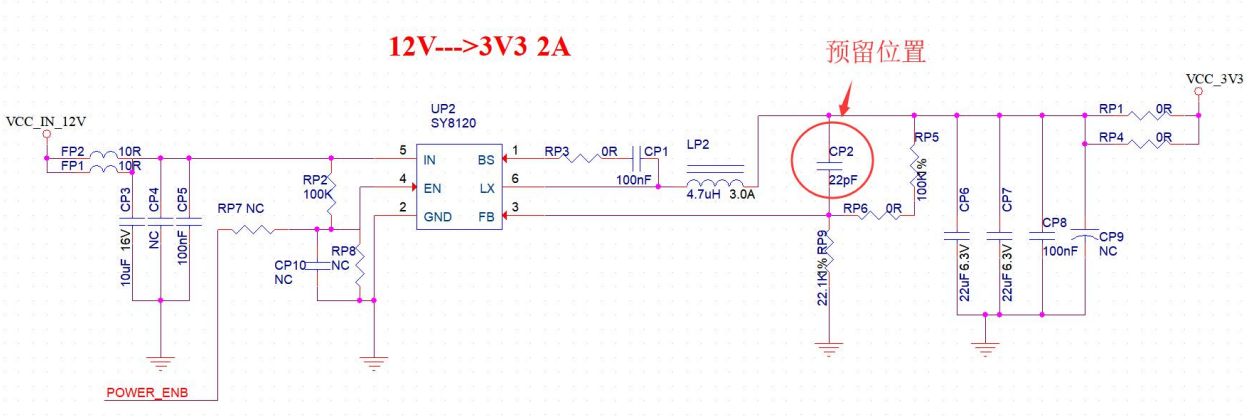
(2) GPIO18 needs to add an external pull-up resistor as U1RXD.

2. Antenna layout requirements

(1) For the installation position on the motherboard, the following two methods are recommended:
Solution 1: Put the module on the edge of the motherboard, and the antenna area extends out of the edge of the motherboard.
Solution 2: Put the module on the edge of the motherboard, and hollow out an area at the antenna position on the edge of the motherboard.
(2) In order to meet the performance of the onboard antenna, it is forbidden to place metal parts around the antenna, away from high-frequency components.

3. Power supply
(1) Recommended 3.3V voltage, peak current above 500mA
(2) It is recommended to use LDO for power supply; if DC-DC is used, the ripple is recommended to be controlled within 30mV.
(3) It is recommended to reserve the position of dynamic response capacitor for DC-DC power supply circuit, which can optimize the output ripple when the load changes greatly.
(4) It is recommended to add ESD devices to the 3.3V power interface。





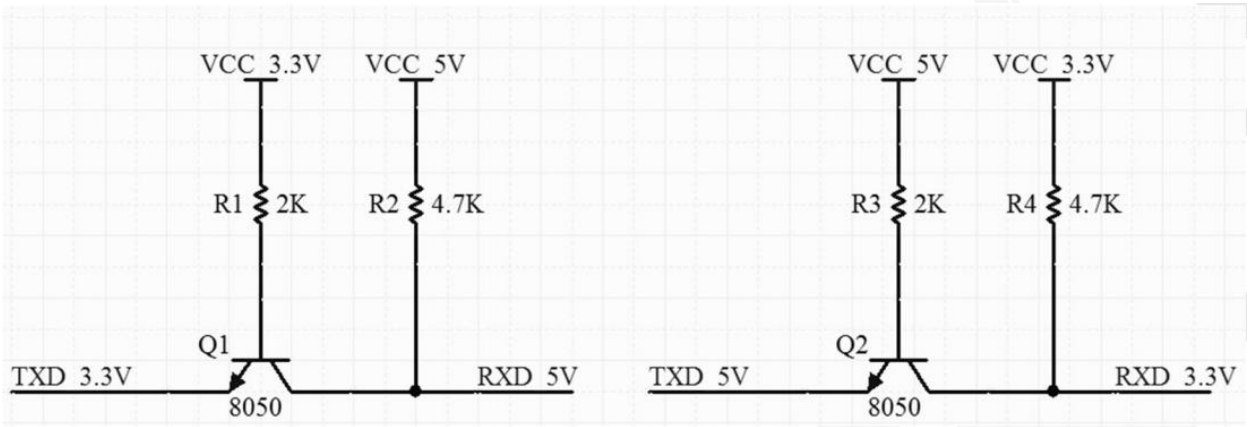
4. Use of GPIO port

(1) There are some GPIO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This can suppress overshoot and make the levels on both sides more stable. It is helpful for EMI and ESD.

(2) For the pull-up and pull-down of special IO ports, please refer to the instructions in the specification, which will affect the startup configuration of the module.

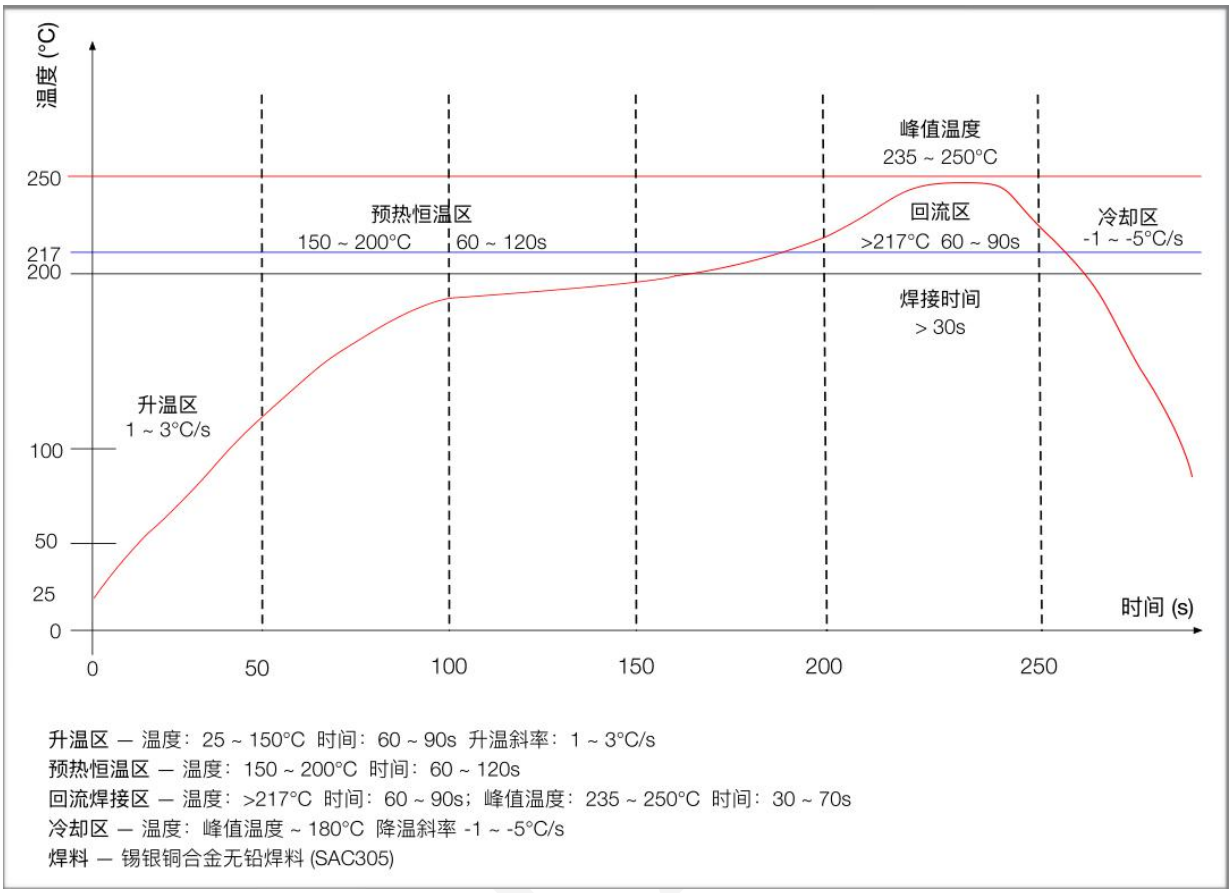
(3) The IO port of the module is 3.3V. If the main control and the IO level of the module do not match, a level conversion circuit needs to be added.

(4) If the IO port is directly connected to a peripheral interface, or a terminal such as a pin header, it is recommended to reserve an ESD device near the terminal of the IO trace.



Pic Level conversion circuit

7.Reflow profile



升温区 — 温度：25 ~ 150°C 时间：60 ~ 90s 升温斜率：1 ~ 3°C/s
预热恒温区 — 温度：150 ~ 200°C 时间：60 ~ 120s
回流焊接区 — 温度：>217°C 时间：60 ~ 90s；峰值温度：235 ~ 250°C 时间：30 ~ 70s
冷却区 — 温度：峰值温度 ~ 180°C 降温斜率 -1 ~ -5°C/s
焊料 — 锡银铜合金无铅焊料 (SAC305)

8.Package

As shown below, the packaging of ESP-12H is braid.

9.Contact us

Official website：https://www.ai-thinker.com

Development DOCS：https://docs.ai-thinker.com

Official forum：http://bbs.ai-thinker.com

Sample purchase：https://ai-thinker.en.alibaba.com/

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