Ai-WB2-01N Specification

Version V1.0.1

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Document resume

Version	Date	Develop/revise content	Edition	Approve
V1.0.0	2023.2.3	First Edition	Jinran Xiao	NingGuan
V1.0.1	2023.3.16	New test data, change the Flash size and rendering diagram	Jinran Xiao	NingGuan

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Content

1. Product Overview 4
1.1. Characteristic 5
2. Main parameters 6
2.1. Static electricity requirement 6
2.2. Electrical characteristics 7
2.3. Wi-Fi RF Performance 7
2.4. BLE RF Performance 8
2.5. Power 8
3. Appearance Dimensions 9
4. Pin Definition 10
5. Schematic 12
6. Antenna parameters 13
6.1. Schematic diagram of the antenna test prototype 13
6.2. Antenna S parameter 14
6.3. Antenna Gain and Efficiency 14
6.4. Antenna pattern 15
6.5. RF OTA parameterss 16
7. Design Guidance 17
7.1. Application circuit 17
7.2. Recommend PCB footprint size 17
7.3. Antenna layout requirements 18
7.4. Power supply 18
7.5. GPIO 19
8. Storage conditions 20
9. Reflow welding curve diagram 20
10. Product Packaging Information 21
11. Contact us 21
Disclaimer and copyright notice 22
Notice 22

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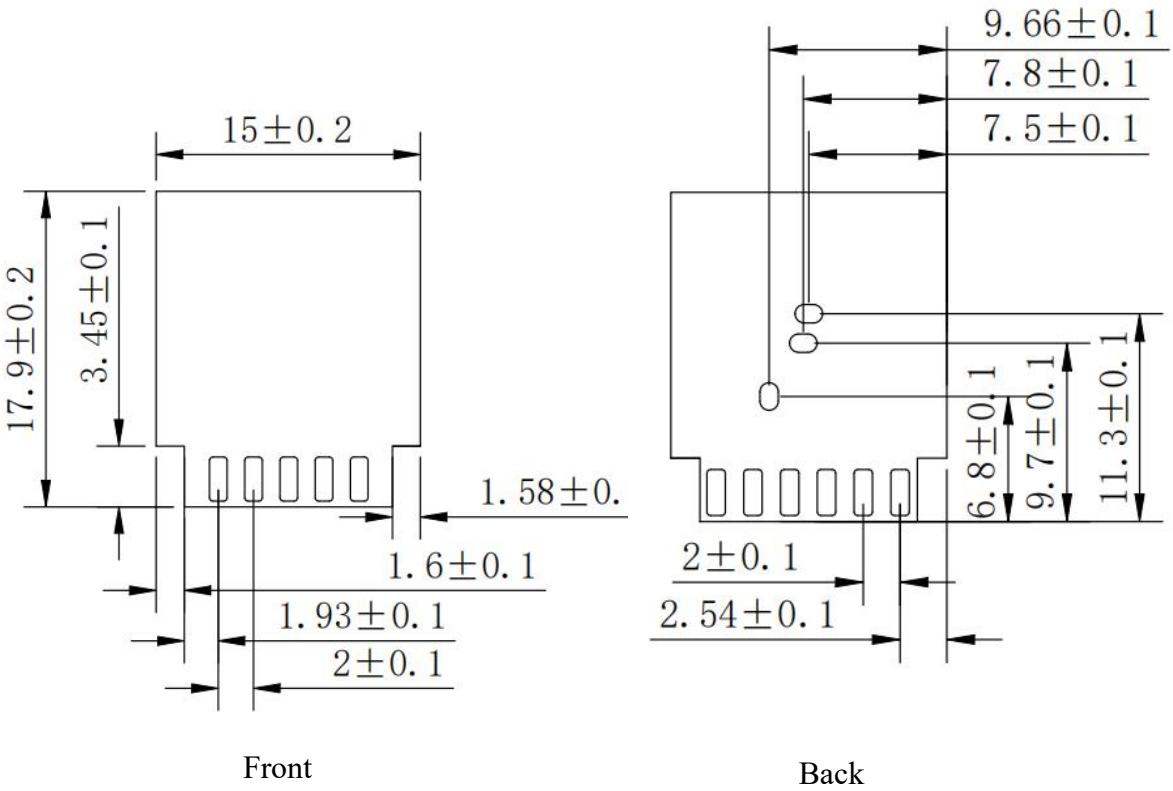
3. Appearance Dimensions

Front Back

Figure 3 Appearance diagram (Rendering figure is for reference only,subject to physical objects)



Front Back

Figure 4 Dimension diagram（单位：mm）

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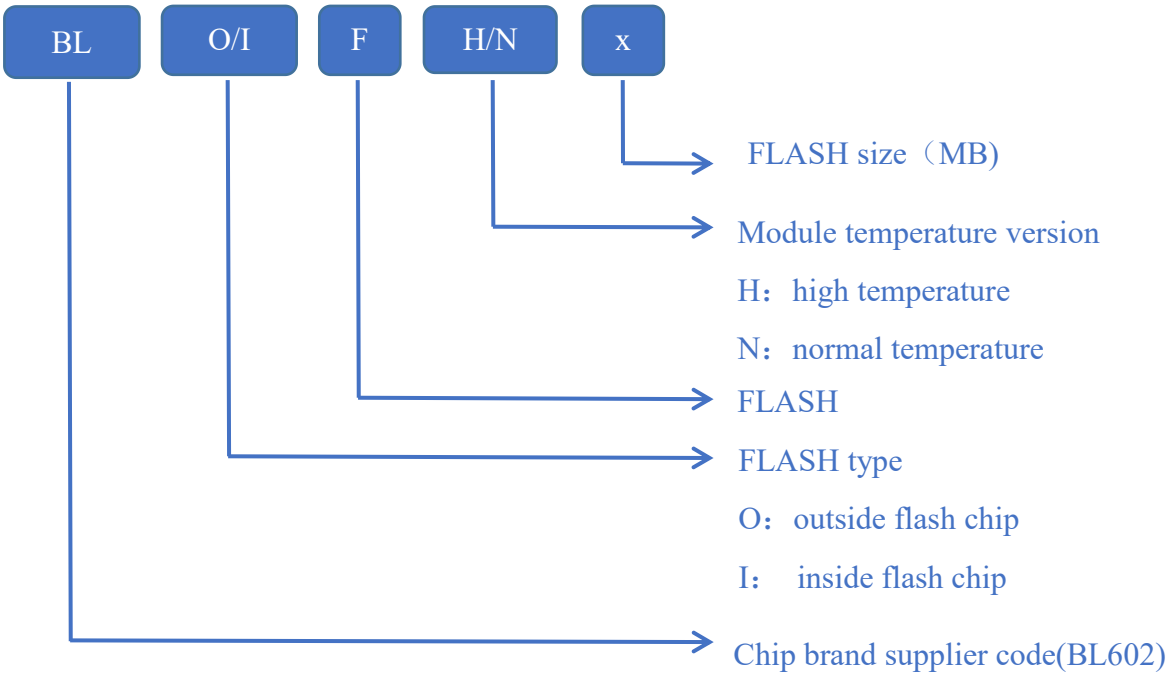

Figure 5 Shield printing information

4. Pin Definition

Ai-WB2-01N module is connected with a total of 14 pins, as shown in the pin schematic diagram, pin function definition table is the interface definition.

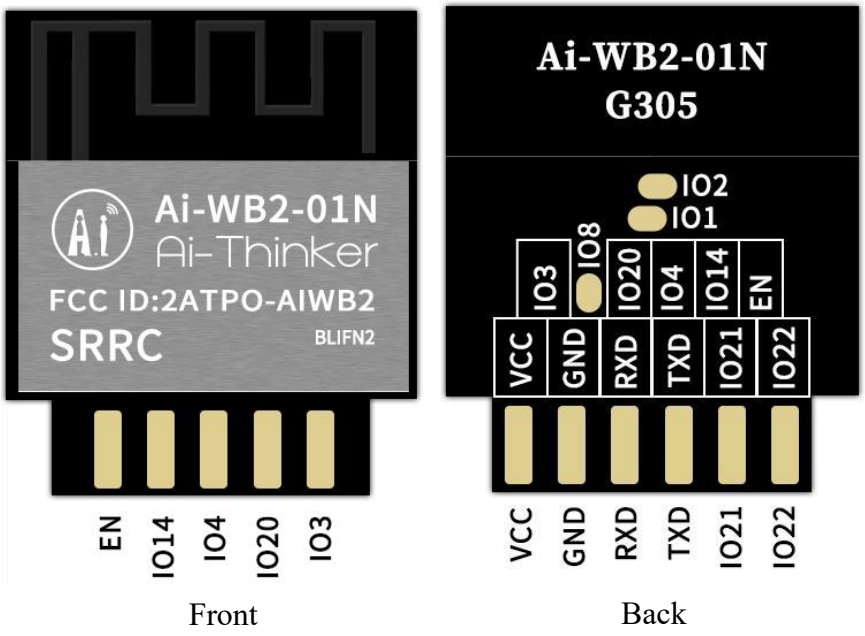

Figure 6 Schematic diagram of module pins

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Table 6 Pin function definition table

No.	Na	Function
1	VCC	3.3V power supply; It is recommended that the output current of the external power supply be higher than 500mA
2	IO3	GPIO3/SPI_SCLK/IIC_SDA/PWM_CH3
3	GN	Ground
4	IO20	GPIO20/SPI_MOSI/MISO/IIC_SCL/PWM_CH0
5	RXD	RXD/GPIO7/SPI_SCLK/IIC_SDA/PWM_CH2
6	IO4	GPIO4/SPI_MOSI/MISO/IIC_SCL/PWM_CH4/ADC_CH1
7	TXD	TXD/GPIO16/SPI_MOSI/MISO/IIC_SCL/PWM_CH1
8	IO14	GPIO14/SPI_SS/IIC_SCL/PWM_CH4/ADC_CH2/DAC_B
9	IO21	GPIO21/SPI_MOSI/MISO/IIC_SDA/PWM_CH1
10	EN	Default chip enable pin, active-high
11	IO22	GPIO22/SPI_SS/IIC_SCL/PWM_CH2
Test point	IO8	Bootstrap/GPIO8/SPI_MOSI/MISO/IIC_SCL/PWM_CH3
Test point	IO1	GPIO1/SPI_MOSI/MISO/IIC_SDA/PWM_CH1
Test point	IO2	GPIO2/SPI_SS/IIC_SCL/PWM_CH2

Note:
GPIO8 as Bootstrap, when the module enters burning mode, the power moment is high level; when the power moment is low level, the module starts normally

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5. Schematic

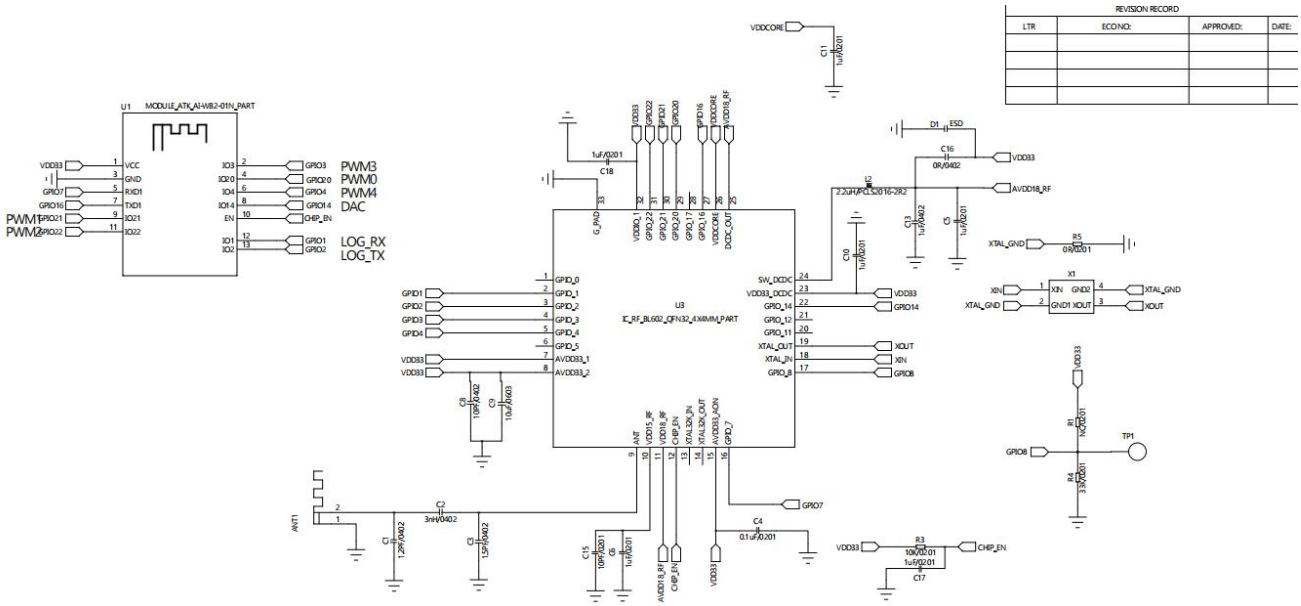

Figure 7 Module schematic

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6. Antenna parameters

6.1. Schematic diagram of the antenna test prototype

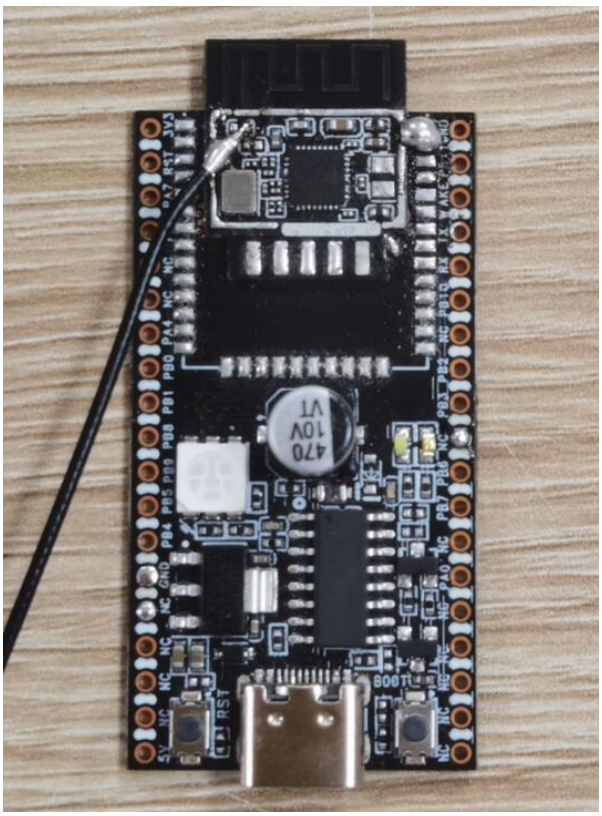

Figure 8 Schematic diagram of the antenna test prototype

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6.2. Antenna S parameter

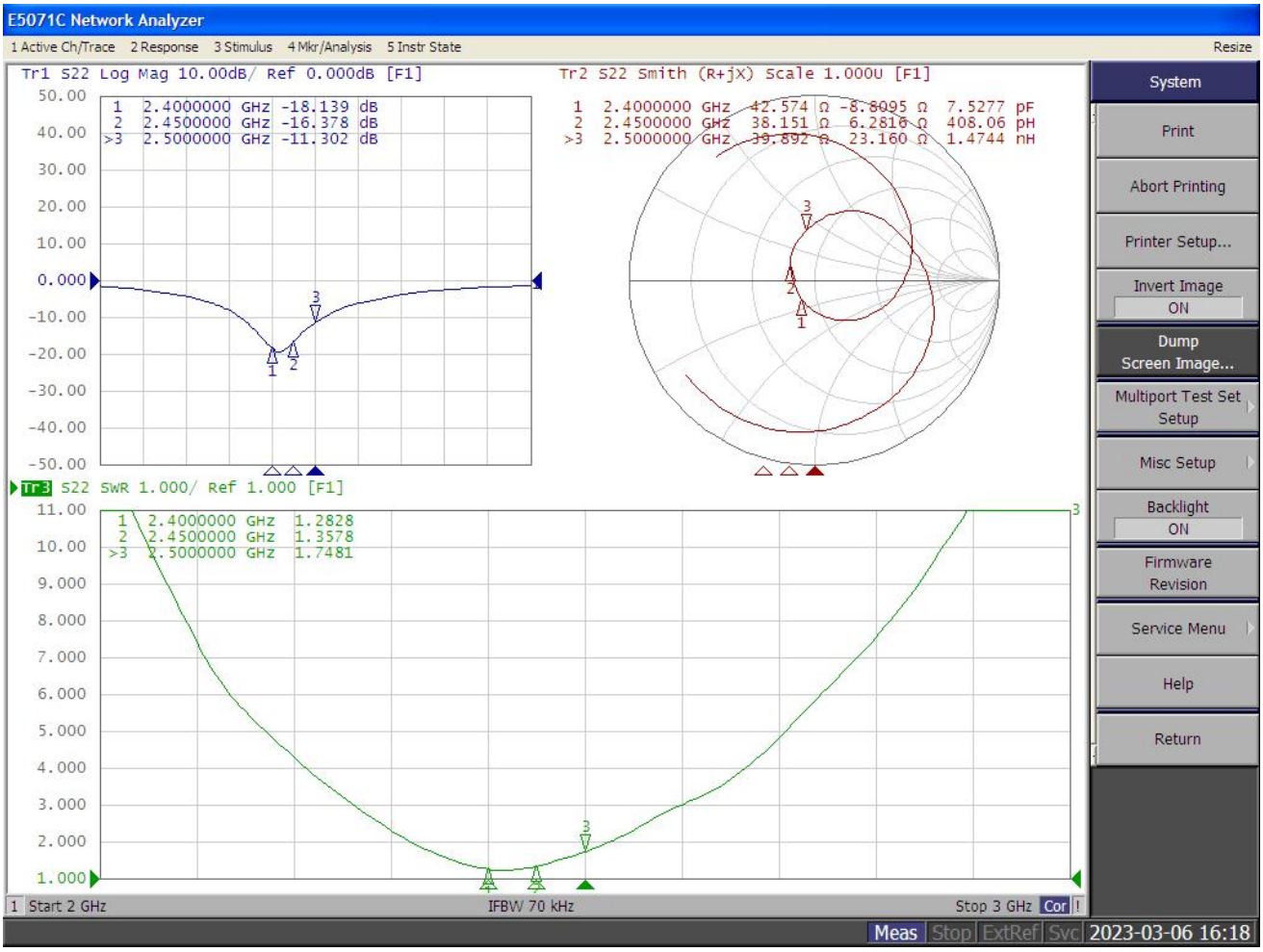

Figure 9 Antenna S parameters

6.3. Antenna Gain and Efficiency

Table 7 Antenna Gain and efficiency

Frequency ID	1	2	3	4	5	6	7	8	9	10	11
Frequency(MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Gain (dBi)	1.72	1.68	1.71	1.89	2.08	2.06	2.08	2.03	1.96	1.90	2.00
Efficiency (%)	50.25	49.60	49.19	50.19	52.19	52.11	52.58	52.16	51.67	50.86	50.88

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6.4. Antenna pattern

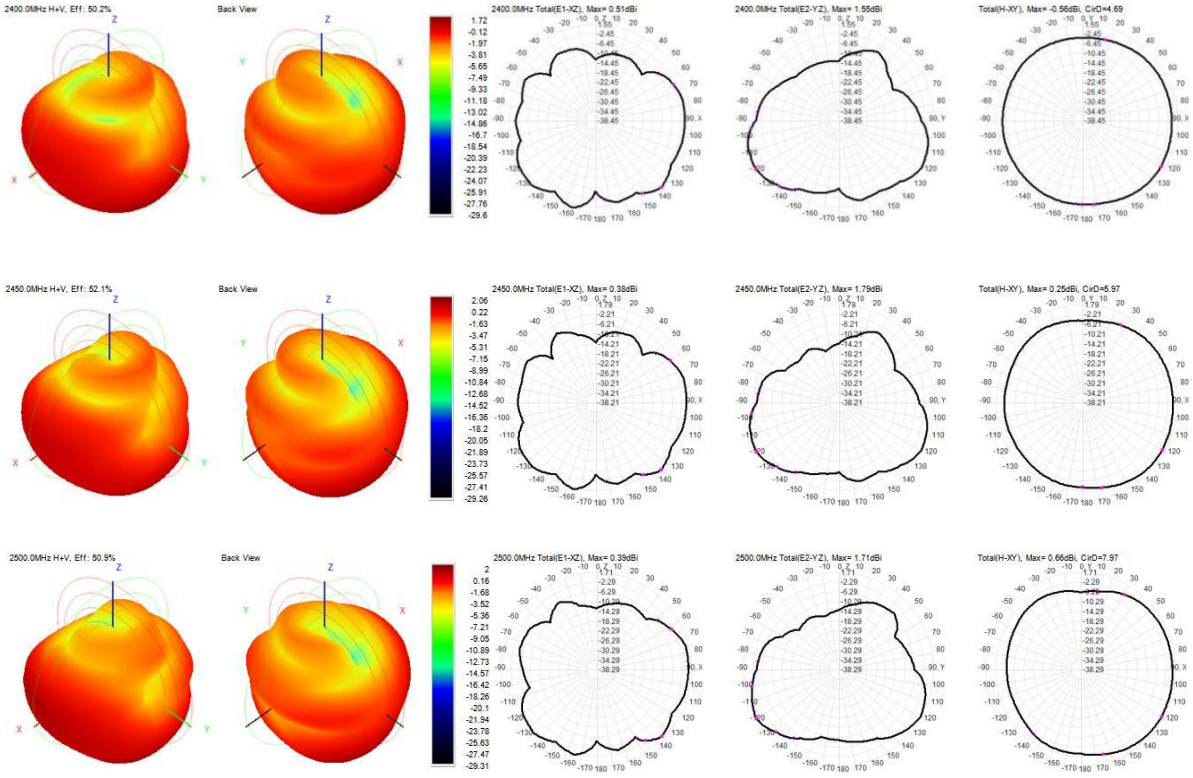

Figure 10 Antenna pattern

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6.5. RF OTA parameterss

Table 8 RF OTA parameters

Item	Mode	Rate(Mbps)	Channel	Fre.(MHz)	Data(dBm)
TRP	11b	11	1	2412	16.97
			6	2437	15.80
			13	2472	15.22
	11g	54	1	2412	14.72
			6	2437	13.55
			13	2472	12.91
	HT20	MCS7	1	2412	14.60
			6	2437	13.28
			13	2472	12.49
TIS	11b	11	1	2412	-84.25
			6	2437	-82.28
			13	2472	-82.15
	11g	54	1	2412	-71.00
			6	2437	-70.57
			13	2472	-70.26
	HT20	MCS7	1	2412	-66.76
			6	2437	-64.90
			13	2472	-64.37

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7. Design Guidance

7.1. Application circuit

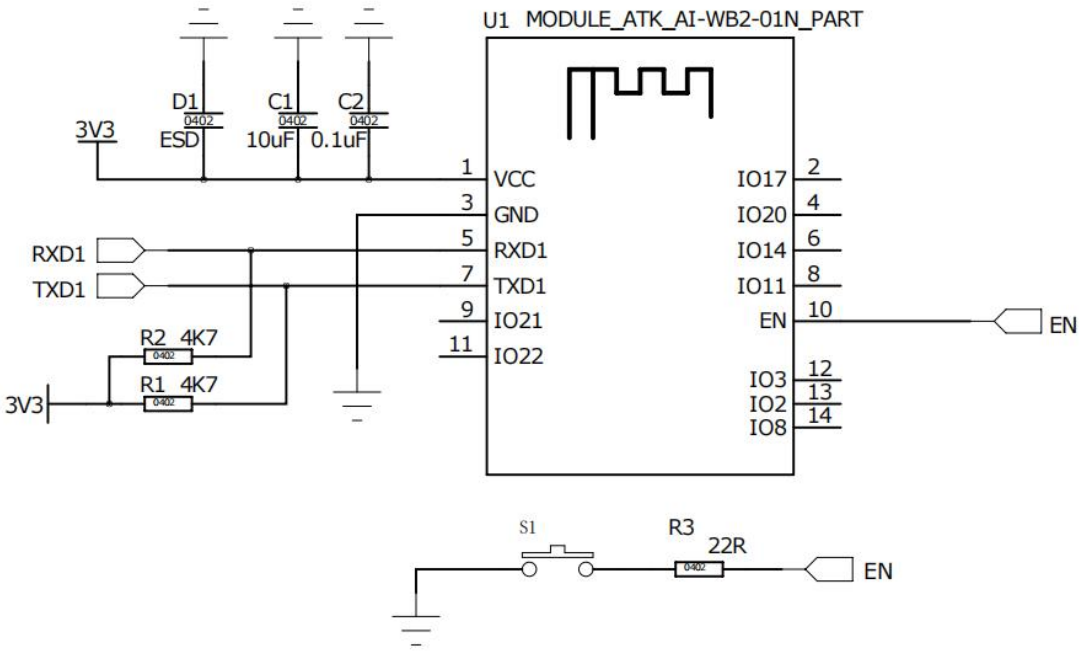

Figure 11 Application circuit diagram

- If the IO port is used as PWM, it is recommended to reserve a 4.7K pull-down resistor around the module. Especially in the application of light control, it can prevent the flashing light phenomenon at the moment of power-on start.
- The 8/NC pin, which are not available by default.If you need to use it, please contact Ai-Thinker.

7.2. Recommend PCB footprint size

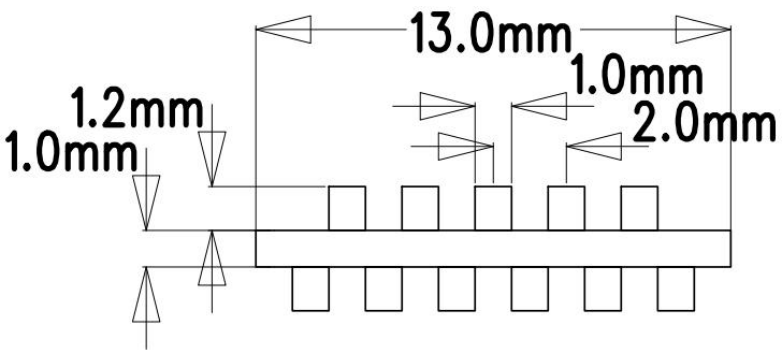

Figure 12 Recommend PCB footprint size

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7.3. Antenna layout requirements

- The following two methods are recommended for the installation position on the mainboard:

Option 1: put the module on the edge of the motherboard, and the antenna area extends out of the edge of the motherboard.

Option : put the module on the edge of the motherboard, the edge of the motherboard at the antenna position hollowed out an area.

- In order to meet the performance of onboard antenna, it is forbidden to place metal parts around the antenna and keep away from high frequency devices.

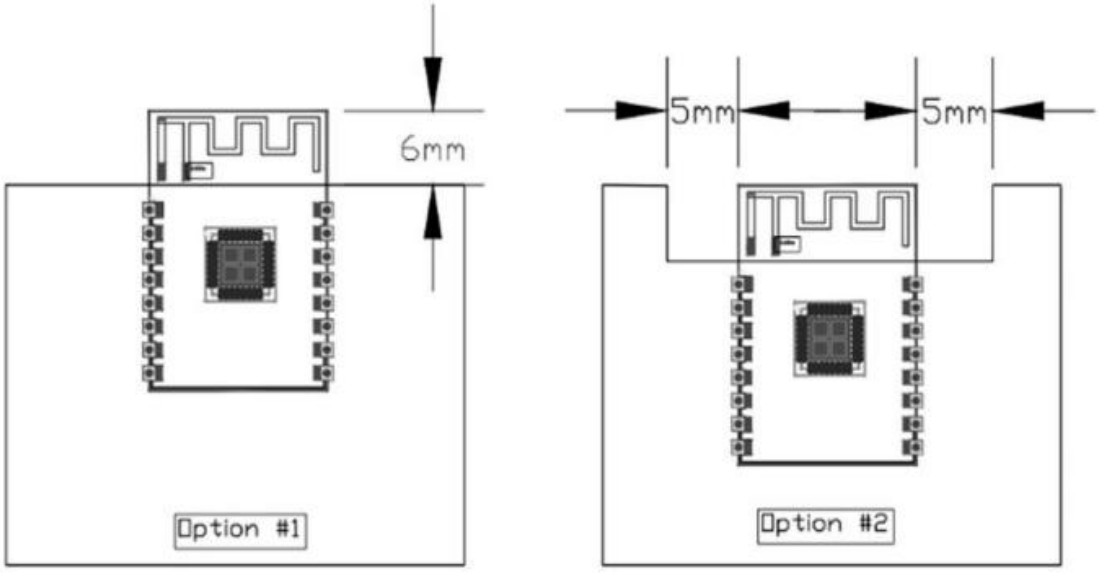

Figure 13 Antenna layout diagram

7.4. Power supply

- Recommended 3.3V voltage,peak current over 500mA.
- Power supply is recommend to use LDO; if the DC-DC is used, the ripple is recommended to be controlled within 30mV
- DC-DC power supply circuit proposes to reserve the dynamic response capacitance to optimize the output ripple with large load changes.
- It is recommended to add ESD devices to the 3.3V power interface.

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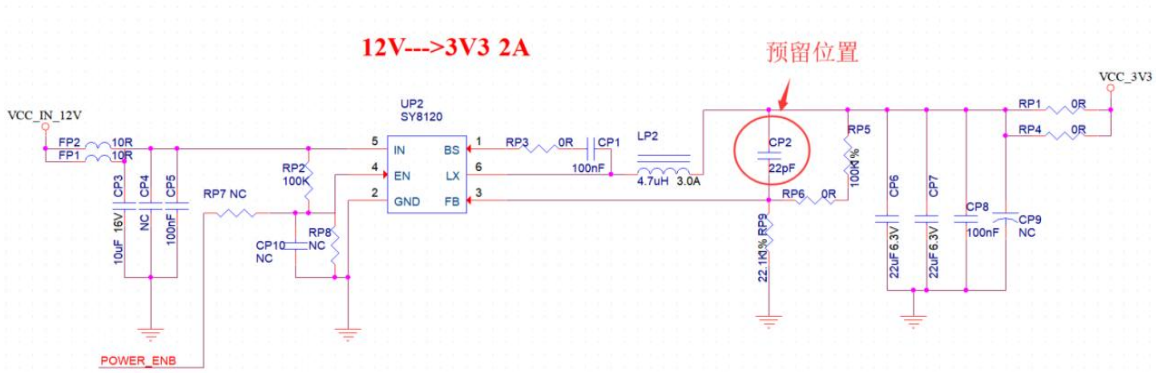

Figure 14 DC-DC step-down circuit diagram

7.5. GPIO

- There are some IO ports on the periphery of the module. If you need to use it, it is recommended to connect a 10-100 ohm resistor in series with the IO port. This inhibits overshoot and makes both sides level more stable. It is helpful for EMI and ESD.
- For special I/O ports to be pulled up and down, refer to the direction for use in the specifications, which may affect the module start-up configuration.
- The IO port of the module is 3.3V. If the IO level of the main control and the module do not match, a level convert circuit needs to be added.
- If the I/O port is directly connected to a peripheral port or terminals, for example, a pin row, reserve an ESD device near the terminal of the I/O cable.

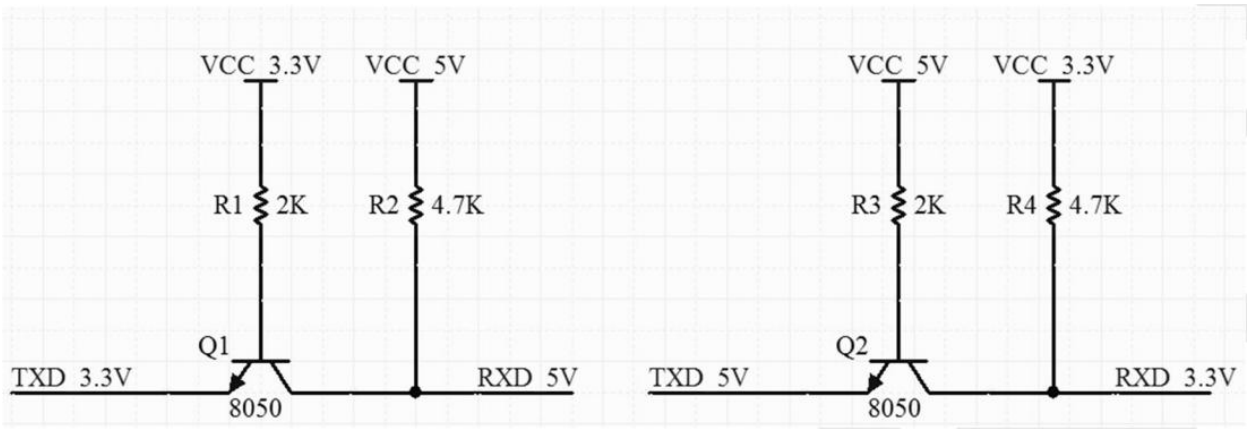

Figure 15 Level convert circuit

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8. Storage conditions

Products sealed in moisture-proof bags should be stored in a non-condensing atmosphere of <40 ° C /90%RH.

The module has a moisture sensitivity rating of MSL 3.

After the vacuum bag is opened, it must be used within 168 hours at 25±5℃/60%RH, otherwise it needs to be baked before it can be put on line again.

9. Reflow welding curve diagram

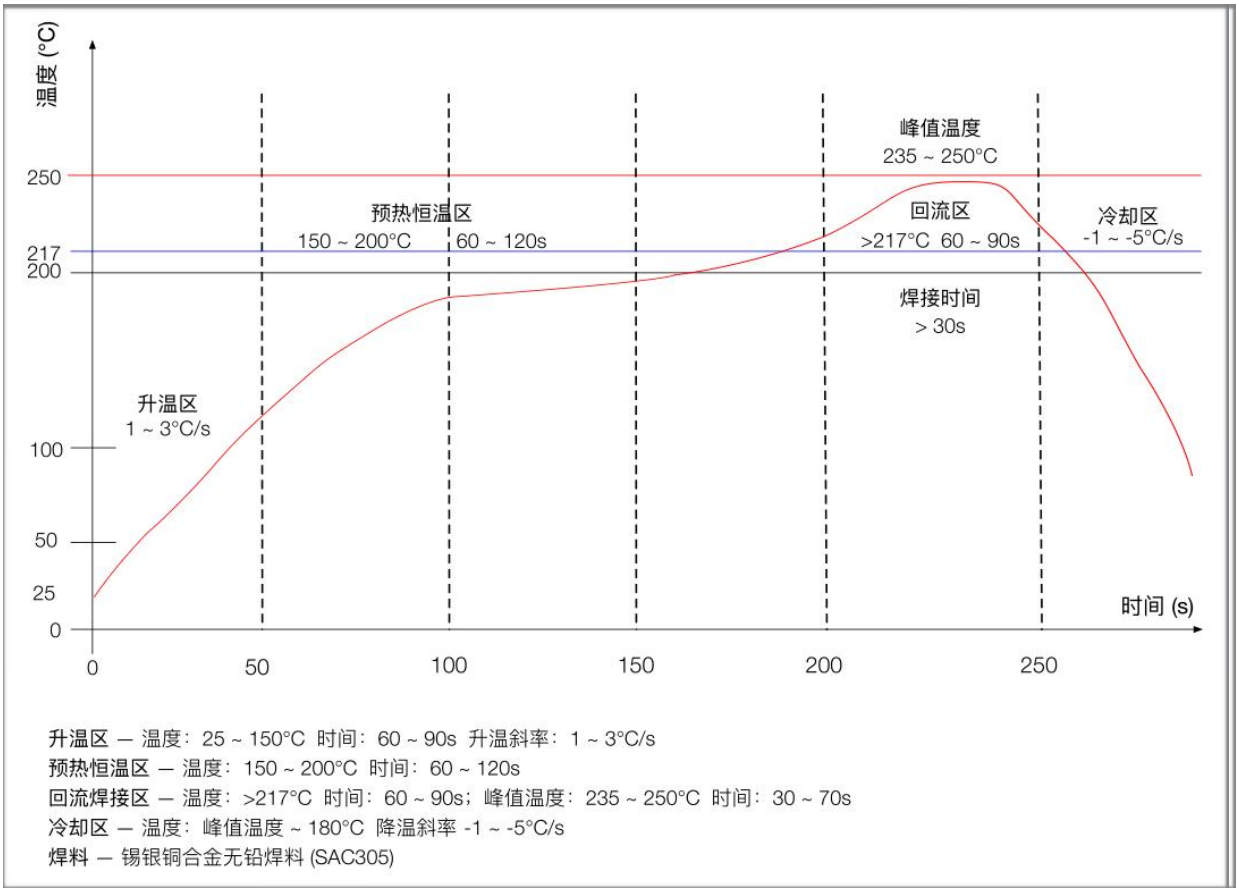

Figure 16 Reflow welding diagram

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10.Product Packaging Information

Ai-WB2-01N module was packaged in a tape, 1000pcs/reel. As shown in the below image:

Figure 17 Package and packing diagram

11.Contact us

Ai-Thinker official website　　Office forum　　Develop DOCS

LinkedIn　　Tmall shop　　Taobao shop　　Alibaba shop

Technical support email：support@aithinker.com

Domestic business cooperation：sales@aithinker.com

Overseas business cooperation：overseas@aithinker.com

Company Address：Room 403,408-410, Block C, Huafeng Smart Innovation Port, Gushu 2nd Road, Xixiang, Baoan District, Shenzhen.

Tel：+86-0755-29162996

WeChat mini program

WeChat official account

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