GC0328C

1/6.5 " VGA CMOS Image Sensor

Datasheet

V1.1

2018-08-27

GalaxyCore Inc.

Ordering Information

- **GC0328C-C20Y0**
  (Colored, 20PIN-CSP)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
V 1.0	*2014-09-30*	*Document Release*	*AE Dept.*
V 1.1	*2018-08-27*	*Modify Ordering Information Product ID From GC0328 To GC0328C-C20Y0*	*QA Dept*

Content

1. Sensor Overview

1.1 General Description

The GC0328C features 640V x 480H resolution with 1/6.5-inch optical format, and 4-transistorpixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.

The full scale integration of high-performance and low-power functions makes the GC0328C fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The product is capable of operating at up to 30 fps at 24MHZ clock in VGA mode, which can be completely controlled by user over image quality and data format.

1.2 Features

- Standard optical format of 1/6.5 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Support adjusting Voltage of IO
- Windowing support
- Horizontal /Vertical mirror
- Image processing module
- Package: CSP/wafer

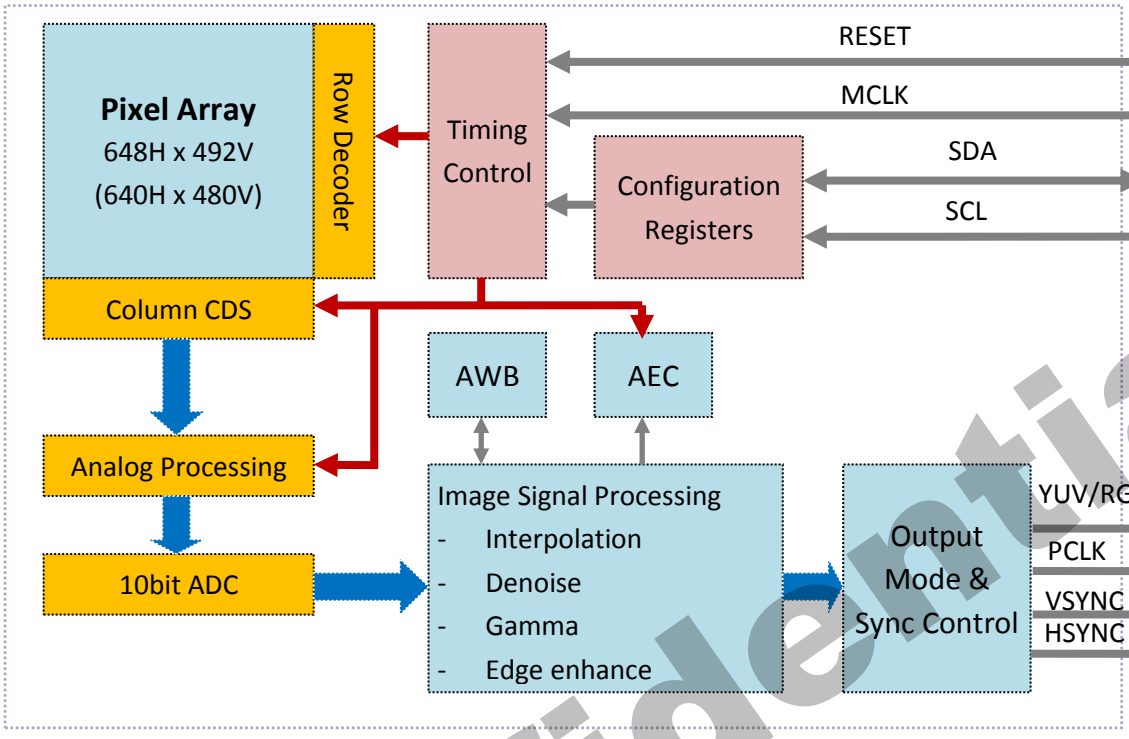
1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

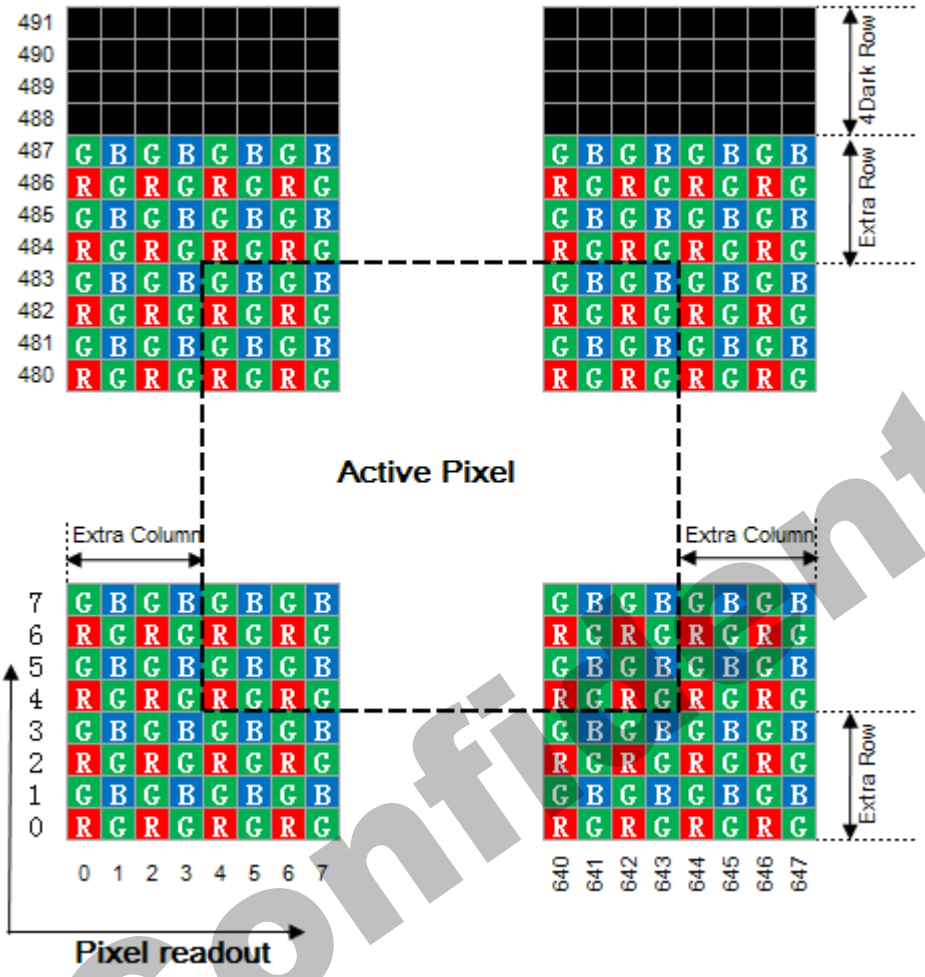
Parameter	Typical value
Optical Format	1/6.5 inch
Pixel Size	3.4um x 3.4um
Active pixel array	648 x 488
ADC resolution	10 bit ADC
Max Frame rate	30fps@24Mhz,VGA
Power Supply	AVDD28: 2.7 ~ 3.0V IOVDD: 1.7 ~ 3.0V
Power Consumption	80mW @30fps VGA <50μA @standby
SNR	41dB
Dark Current	25mV @ 60℃
Sensitivity	1.8V/（Lux.sec）
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	27 (linear)
Package type	CSP/Wafer

1.5 Block Diagram



GC0328C has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, denoise, and color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

1.6 Pixel Array



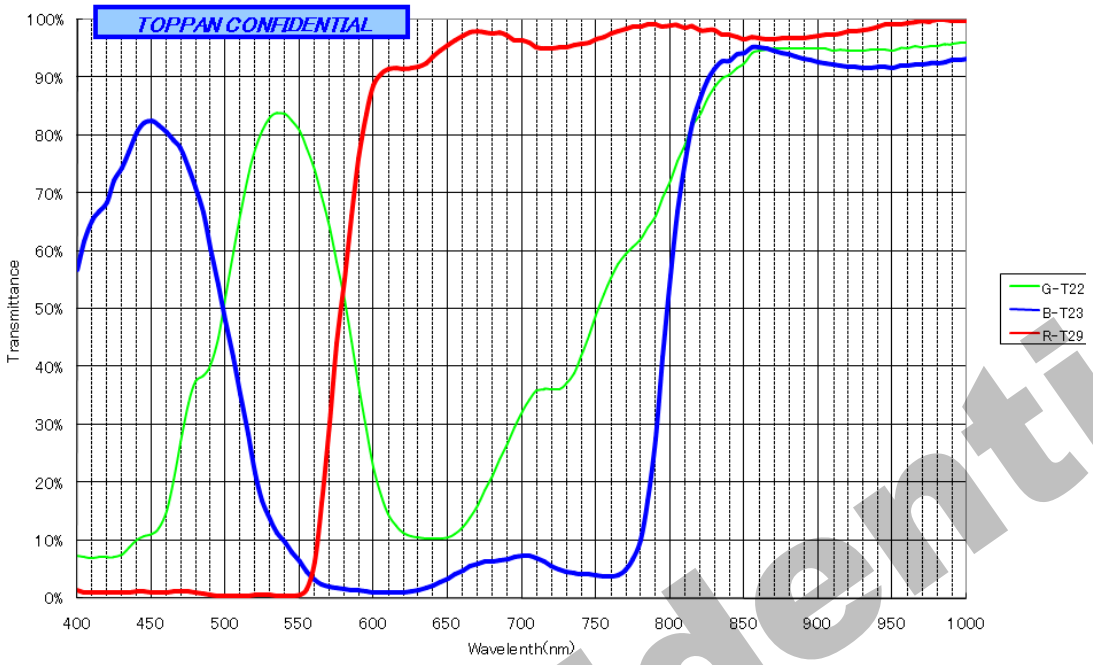
Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is readout from 0 to 647. If flip in column, column is read out from 647 to 0.

If no flip in row, row is readout from 0 to 487. If flip in row, row is read out from 487 to 0.

2. Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



3. Two-wire Serial Bus Communication

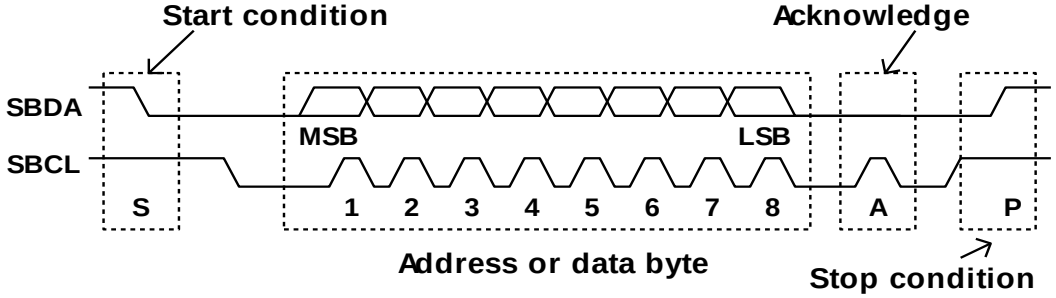
GC0328C Device Address:

serial bus write address = 0x42H, serial bus read address = 0x43H

3.1 Protocol

The host must perform the role of a communications master and GC0328C acts as either a slave receiver or transmitter. The master must do

- Generate the **Start(S)/Stop(P)** condition
- Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	NA	P

Incremental Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data(1)	A	……	Data(N)	NA	P

Notes:

From master to slave

From slave to master

S: Start condition

P: Stop condition

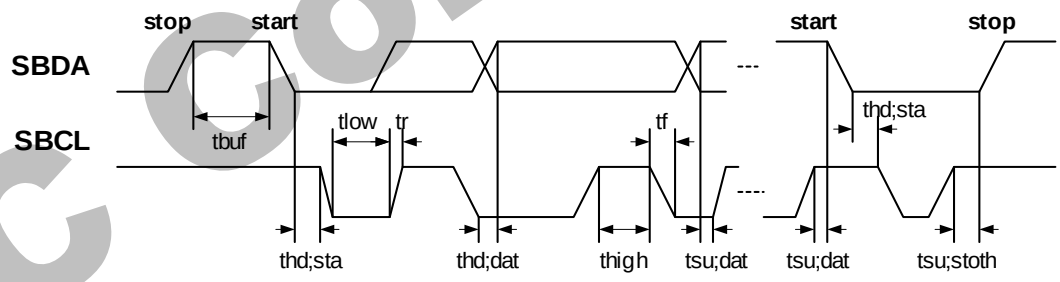
A: Acknowledge bit

NA: No acknowledge

Register Address: Sensor register address

Data: Sensor register value

3.2 Serial Bus Timing



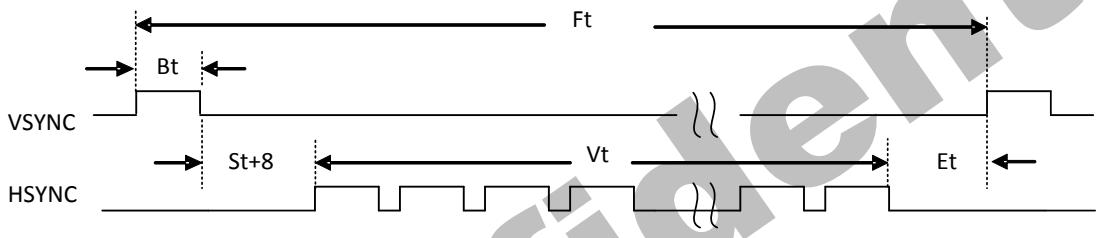
Parameter	Symbol	Min.	Max.	Unit
SBCL clock frequency	fscl	0	400	KHz
Bus free time between a stop and a start	tbuf	1.2	*	μs
Hold time for a repeated start	thd;sta	1.0	*	μs
LOW period of SBCL	tlow	1.2	*	μs
HIGH period of SBCL	thigh	1.0	*	μs
Set-up time for a repeated start	tsu;sta	1.2	*	ns
Data hold time	thd;dat	1.3	*	ns
Data Set-up time	tsu;dat	250	*	ns

Rise time of SBCL, SBDA	tr	*	250	ns
Fall time of SBCL, SBDA	tf	*	300	ns
Set-up time for a stop	tsu;sto	1.2	*	μs
Capacitive load of bus line (SBCL, SBDA)	Cb	*	*	pf

4. Application

4.1 Timing

Suppose VSYNC is LOW active and HSYNC is HIGH active, and output format is YCbCr/RGB565, then the timing of VSYNC and HSYNC is shown below:



Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, VSYNC no active time.

St -> Start time, setting by register P0:0x12.

Et –> End time, setting by register P0:0x13.

Vt -> valid line time. VGA is 480, Vt = win_heigh t- 8, win_height is setting by register P0:0x0d & P0:0x0e (488).

When exp_time <= win_height + VB, Bt=VB – St - Et. Frame rate is controlled by window_height + VB.

When exp_time > win_height + VB, Bt=exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width + 4.

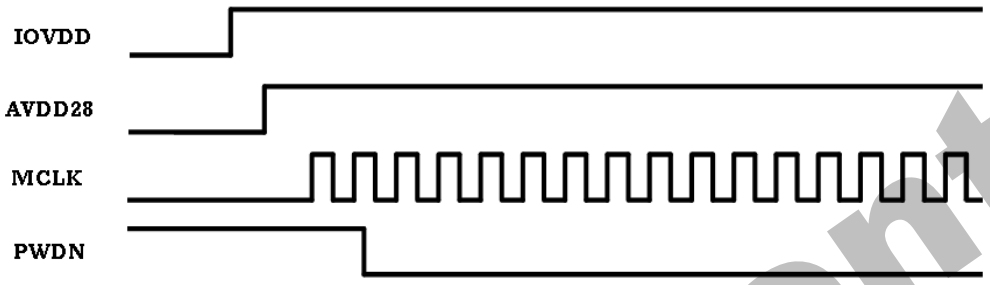
Hb –> HBlank or dummy pixel, Setting by register P0:0x05 and P0:0x06.

Sh_delay -> Setting by register P0:0x11.

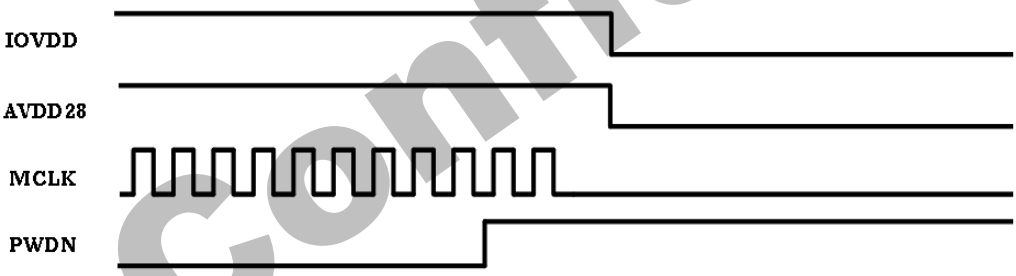
win_width -> Setting by register P0:0x0f and P0:0x10, win_width = 640, final_output_width + 8. So for VGA, we should set win_width as 648.

4.2 Power on/off sequence

4.2.1 Power On Sequence



4.2.2 Power Off Sequence



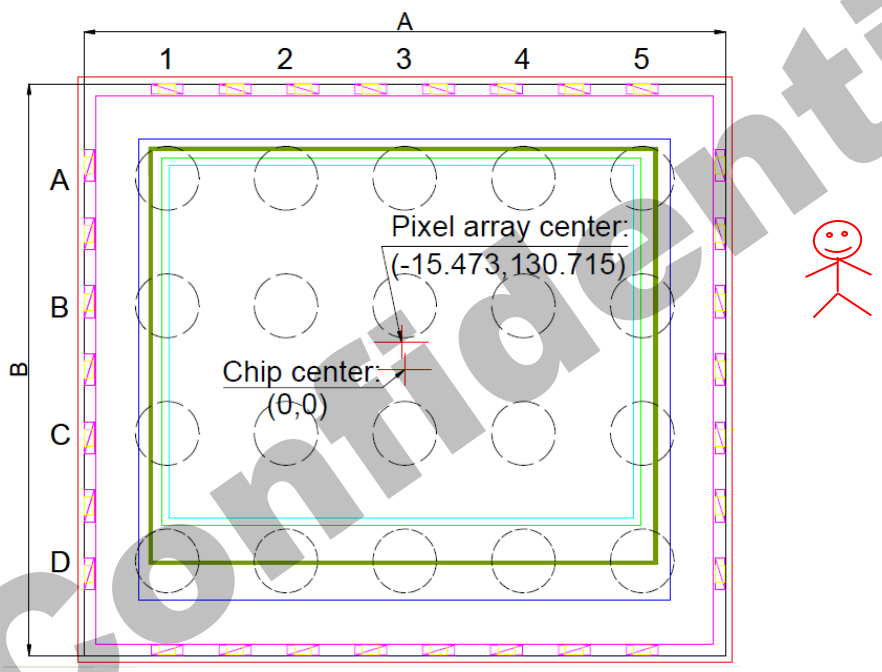
5. DC Parameters

Symbol	Parameter		Min	Typ	Max	Unit
SUPPLY						
V_{AVDD28}		Power Supply	2.7	2.8	3.0	V
V_{IOVDD}		Power Supply(Digital I/O)	1.7	1.8	3.0	V
I_{AVDD28}		Active(Operating) Current	--	8	24	mA
I_{IOVDD}	**1.8V**		--	12	24	mA
	2.8V		--	15	24	mA
$I_{DDS-PWDN}$		Standby Current	--	35	50	uA
Digital Input(Typical conditions: AVDD28 = 2.8V，IOVDD = 1.8V)						
V_{IH}		Input voltage HIGH	1.4			V

V_{IL}	Input voltage LOW			0.6	V
Digital Input(Typical conditions: AVDD28 = 2.8V，IOVDD = 1.8V)					
V_{OH}	Output voltage HIGH	1.6			V
V_{OL}	Output voltage LOW			0.2	V

6. Pin Description

6.1 GC0328C CSP package Top view (unit: μm)



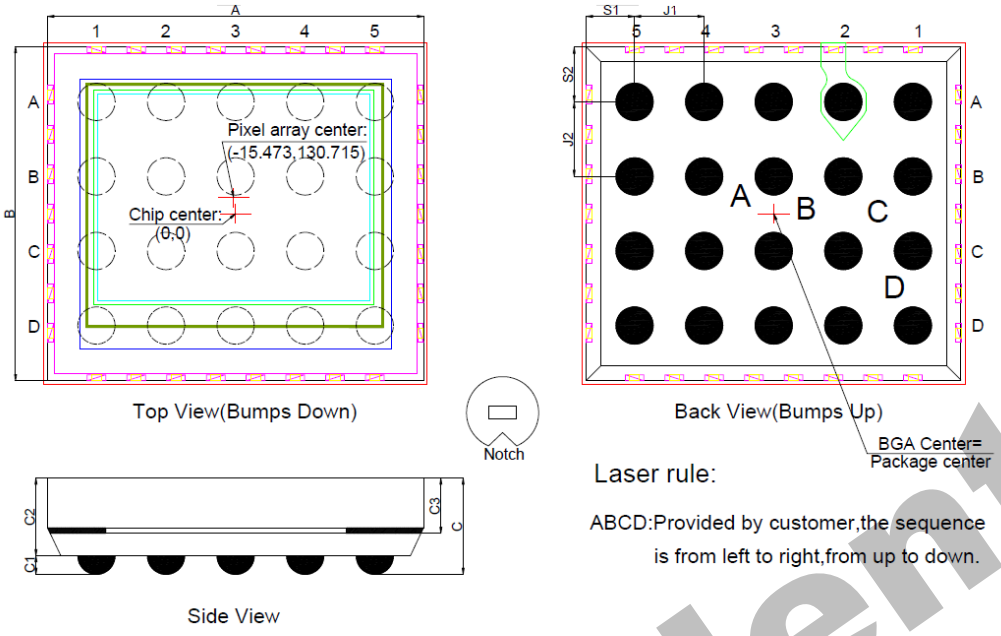
6.2 CSP ball description

	1	2	3	4	5
A	AVDD28	SBCL	VSYNC	D<7>	D<6>
B	AGND	SBDA	HSYNC	D<5>	DGND
C	TXLOW	INCLK	D<1>	PCLK	D<4>
D	PWDN	D<0>	D<2>	D<3>	IOVDD

6.3 GC0328C chip pin description

Pin	Name	Pin Type	Function
A1	AVDD28	Power	Main power supply, 2.7~3.0V, Please connect capacity to ground.
A2	SBCL	Input	Two-wire serial bus, clock
A3	VSYNC	Output	VSYNC output
A4	D<7>	Output	YUV/RGB data output bit[7]
A5	D<6>	Output	YUV/RGB data output bit[6]
B1	AGND	Ground	Chip ground
B2	SBDA	I/O	Two-wire serial bus, data
B3	HSYNC	Output	HSYNC output
B4	D<5>	Output	YUV/RGB data output bit[5]
B5	DGND	Ground	Chip ground
C1	TXLOW	Power	Internal analog voltage. Please connect capacity to ground.
C2	INCLK	Input	Main clock
C3	D<1>	Output	YUV/RGB data output bit[1]
C4	PCLK	Output	Pixel clock output
C5	D<4>	Output	YUV/RGB data output bit[4]
D1	PWDN	Input	Sensor power down control: 0: normal work 1: standby
D2	D<0>	Output	YUV/RGB data output bit[0]
D3	D<2>	Output	YUV/RGB data output bit[2]
D4	D<3>	Output	YUV/RGB data output bit[3]
D5	IOVDD	Power	Power Supply for I/O circuits, 1.7~3.0V. Please connect capacity to ground.

6.4 CSP package mechanical drawing (unit: μm)



6.5 CSP package description

Description	Symbol	Nominal	Min.	Max.
		Millimeters		
Package Body Dimension X	A	3.034	3.009	3.059
Package Body Dimension Y	B	2.700	2.675	2.725
Package Height	C	0.745	0.685	0.805
Ball Height	C1	0.160	0.130	0.190
Package Body Thickness	C2	0.585	0.540	0.630
Thickness from top glass surface to wafer	C3	0.435	0.415	0.455
Ball Diameter	D	0.300	0.270	0.330
Total Ball Count	N	20		
Ball Count X axis	N1	5		
Ball Count Y axis	N2	4		
Pins Pitch X axis	J1	0.560		
Pins Pitch Y axis	J2	0.600		

Edge to Pin Center Distance along X	S1	0.397	0.367	0.427
Edge to Pin Center Distance along Y	S2	0.450	0.420	0.480

7. Register List

SYS_REG

Address	Name	Width	Default Value	R/W	Description
0xf0	**CHIPID**	**8**	**0x9d**	**RO**	**CHIP ID**
0xf1	Pad_setting1	8	0x07	RW	[7] NA [6:4] SYNC_hiz_setting [6] o_pclk_hiz [5] o_HSYNC_hiz [4] o_VSYNC_hiz [3] pad_vb_hiz_mode [2] pclk output enable [1] HSYNC output enable [0] VSYNC output enable
0xf2	Pad_setting2	1	0x01	RW	[7:1] NA [0] data output enable
0xf3	Pad_setting3	8	0x00	RW	[7:6] SYNC pwd mode 00: not pull 01: pull down 10: pull up 11: illegal [5:4] clk pwd mode 00: not pull 01: pull down 10: pull up 11: illegal [3:2] data pwd mode 00: not pull 01: pull down 10: pull up 11: illegal [1] NA [0] Pwd enable 0: pull down 1: not pull
0xfa	clk_div_mode	8	0x00	RW	[7:4] +1, represent the frequency division

					number [3:0] represent the high level in one pulse after frequency division Mclk by Div duty 0x11 2 1:1 0x21 3 1:2 0x22 3 2:1 0x31 4 1:3 0x32 4 2:2 0x33 4 3:1 …
0xfb	device_ID	8	0x42	RO	[7:1] I2C device ID, can write once The default setting is 0x42. [0] NA
0xfc	Clock mode	5	0x16	RW	[7:5] NA [4] digital clock enable [3] NA [2] da25_en [1] da18_en [0] analog pwd
0xfe	Reset related	8	0x00	RW	[7] soft reset [6:5] NA [4] CISCTL_restart_n, restart CISCTL, effective LOW [3:2] NA [1:0] page select 00: REGF 01: REGF1

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	Exposure time high	4	0x00	RO	[7:4] NA [3:0] exposure[11:8],use line processing time as the unit. controlled by AEC if AEC is in function
P0:0x04	Exposure time low	8	0x10	RO	Exposure[7:0], controlled by AEC if AEC is in function
P0:0x05	HB high	4	0x00	RW	[7:4] NA [3:0] HBLANK high bit [11:8]
P0:0x06	HB low	8	0x6a	RW	HBLANK low bit [7:0]

P0:0x07	VB high	4	0x00	RW	[7:4] NA [3:0] VBLANK high bit[11:8]
P0:0x08	VB low	8	0x70	RW	VBLANK low bit[7:0]
P0:0x09	Row start high	1	0x00	RW	[7:1] NA [0] row start high bit[8]
P0:0x0a	Row start low	8	0x00	RW	Row start low bit[7:0]
P0:0x0b	Col start high	2	0x00	RW	[7:2] NA [1:0] Column start high bit[9:8]
P0:0x0c	Col start low	8	0x04	RW	Column start low bit[7:0]
P0:0x0d	Window height high	1	0x01	RW	[7:1] NA [0] Window height high[8]
P0:0x0e	Window height low	8	0Xe8	RW	Window height low[7:0]
P0:0x0f	Window width high	2	0x02	RW	[7:2] NA [1:0] window width high bit[9:8]
P0:0x10	Window width low	8	0x84	RW	Window width low bit[7:0]
P0:0x11	sh_delay	8	0x2a	RW	Sh delay
P0:0x12	Vs_st	8	0x04	RW	number of Row time from frame start to first HSYNC valid
P0:0x13	VS_et	8	0x04	RW	number of Row time from last HSYNC valid to frame end Notice the relation with VB, VB > vs_st+vs_et
P0:0x14	Reserved	8	0xc2	RW	Reserved
P0:0x15	Reserved	8	0x08	RW	Reserved
P0:0x16	Analog gain	8	0x00	RW	[7] Analog gain enable [6:0] NA
P0:0x17	Mirror_Flip	8	0x00	RW	[7] HSYNC always [6:2] Reserved [1] Flip [0] mirror
P0:0x18	Reserved	8	0x0a	RW	Reserved
P0:0x19	Reserved	8	0x05	RW	Reserved
P0:0x1a	Reserved	8	0x00	RW	Reserved
P0:0x1b	Rsh width	8	0x44	RW	Reserved
P0:0x1c	Tsp width	8	0x1d	RW	Reserved
P0:0x1d	Increase win start mode	4	0x00	RW	[7:4] NA [3] increase_win_start_mode [2] custom mode1 [1:0] increase_win_start_frame
P0:0x1e	Analog mode1	8	0x17	RW	[7:2] Reserved [1] clk_delay

					[0] NA
P0:0x1f	Reserved	8	0x00	RW	Reserved
P0:0x20	Reserved	8	0x00	RW	Reserved
P0:0x21	Reserved	8	0x40	RW	Reserved
P0:0x22	Reserved	8	0xba	RW	Reserved
P0:0x23	Reserved	8	0x05	RW	Reserved
P0:0x24	Pad drv	8	0x15	RW	[7:6] NA [5:4] SYNC driver 0 0: 4mA 0 1: 8mA 1 0: 12mA 1 1: 16mA [3:2] data driver 0 0: 4mA 0 1: 6mA 1 0: 10mA 1 1: 12mA [1:0] pclk driver 0 0: 2mA 0 1: 4mA 1 0: 8mA 1 1: 10mA
P0:0x25	Increase win start mode2	8	0x22	RW	Increase win start mode2
P0:0x26	Reserved	4	0x02	RW	Reserved

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Block_enable_1	8	0x5e	RW	[7] middle gamma enable [6] gamma enable [5] CC enable [4] Edge enhancement enable [3] Interpolation enable [2] Noise removal enable [1] Defect removal enable [0] Lens-shading correction enable
P0:0x41	Block_enable_2	7	0x00	RW	[7] NA [6] low light Y enable [5] skin enable [4] skin Y enable

					[3] new skin mode [2] autogray enable [1] Y gamma enable [0] block skin
P0:0x42	AAAA_enable	8	0x00	RW	[7]auto saturation [6] auto EE [5] auto DN [4] auto DD [3] auto LSC [2] ABS enable [1] AWB enable [0] auto Y offset
P0:0x43	special_effect	3	0x00	RW	[7:3] NA [2] edge map [1] CbCr fixed enable [0] Inverse color
P0:0x44	Output_format	8	0x22	RW	[7] NA [6] Smooth Y [5] average neighbor chroma [4:0]output data mode, check details in OUT 5'h00 Cb Y Cr Y 5'h01 Cr Y Cb Y 5'h02 Y Cb Y Cr 5'h03 Y Cr Y Cb 5'h06 RGB 565 5'h07 RGB x555 5'h08 RGB 555x 5'h09 RGB x444 5'h0a RGB 444x 5'h0b BGRG 5'h0c RGBG 5'h0d GBGR 5'h0e GRGB 5'h0f bypass 10bits 5'h11 only Y 5'h12 only Cb 5'h13 only Cr 5'h14 only R 5'h15 only G 5'h16 only B 5'h17 switch odd/even column /row

					to controls output bayer pattern Controls by P0:0x49[7][4] 5'h18 DNDD_out_mode, high 8 5'h19 LSC_out_mode, high 8
P0:0x45	Auto middle gamma mode	2	0x00	RW	[7:2] NA [1] auto gamma mode outdoor [0] auto gamma mode lowlight
P0:0x46	SYNC_mode	8	0x3f	RW	[7] data delay half [6] HSYNC delay half [5] allow pclk around HSYNC [4] allow pclk around VSYNC [3] opclk gated mode [2] opclk polarity 0: invert of isp_2pclk(isp_pclk) 1: same as isp_2pclk(isp_pclk) [1] HSYNC polarity 0: low valid 1: high valid [0] VSYNC polarity 0: low valid 1: high valid
P0:0x49	bypass_mode	8	0x03	RW	[7] odd_even_row_switch [6] Reserved [5] first_second_switch [4] odd_even_col_switch [3] is_8bit_bypass [2] is_10bit_bypass [1:0] bypass which 8bits from 11bit, in is_8bit_bypass mode 11: [10:3]----default 10: [9:2] 01: [8:1] 00: [7:0]
P0:0x4a	Reserved	8	0x81	RW	Reserved
P0:0x4b	Debug mode1	8	0x8b	RW	[7:6] BFF gate mode [5] INBF enable [4] NA [3:2] pipe gate mode [1] AWB gain mode [0] update gain mode
P0:0x4c	Debug mode2	8	0x00	RW	[7] Low Y ratio [6:3] Reserved

					[2] input test image [1] LSC test image [0] test image after EEINTP
P0:0x4d	Reserved	1	0x00	RO	Reserved
P0:0x4f	AEC enable	1	0x00	RW	[0] AEC enable
P0:0x50	Crop_win_mode	1	0x00	RW	[0] crop window mode enable
P0:0x51	Crop _win_y1	2	0x00	RW	[1:0] Crop _win_y1[9:8]
P0:0x52	Crop _win_y1	8	0x00	RW	Crop _win_y1[7:0]
P0:0x53	Crop _win_x1	3	0x00	RW	[2:0] Crop _win_x1[10:8]
P0:0x54	Crop _win_x1	8	0x00	RW	Crop _win_x1[7:0]
P0:0x55	Crop_win_height	1	0x01	RW	[7:1] NA [0] Crop _win_height[8]
P0:0x56	Crop_win_height	8	0xe0	RW	Crop _win_height[7:0]
P0:0x57	Crop_win_width	2	0x02	RW	[7:2] NA [1:0] Crop _win_width[9:8]
P0:0x58	Crop_win_width	8	0x80	RW	Crop _win_width[7:0]
P0:0x59	subsample	8	0x11	RW	[7:4] subsample row ratio [3:0] subsample col ratio
P0:0x5a	Sub mode	6	0x0e	RW	[5] use_or_cut_row 1: use 0: not use [4] use_or_cut_col 1: use 0: not use [3] vacancy_zero_mode [2] remove_00_mode [1] neighbor average mode [0] subsample_extend_opclk
P0:0x5b	Sub_row_N1	8	0x02	RW	[7:4] sub_row_num1 [3:0] sub_row_num2
P0:0x5c	Sub_row_N2	8	0x04	RW	[7:4] sub_row_num3 [3:0] sub_row_num4
P0:0x5d	Sub_row_N3	8	0x00	RW	[7:4] sub_row_num5 [3:0] sub_row_num6
P0:0x5e	Sub_row_N4	8	0x00	RW	[7:4] sub_row_num7 [3:0] sub_row_num8
P0:0x5f	Sub_col_N1	8	0x02	RW	[7:4] sub_col_num1 [3:0] sub_col_num2
P0:0x60	Sub_col_N2	8	0x04	RW	[7:4] sub_col_num3 [3:0] sub_col_num4
P0:0x61	Sub_col_N3	8	0x00	RW	[7:4] sub_col_num5 [3:0] sub_col_num6
P0:0x62	Sub_col_N4	8	0x00	RW	[7:4] sub_col_num7 [3:0] sub_col_num8

BLK

Address	Name	Width	Default Value	R/W	Description
P0:0x27	Blk_mode	8	0x27	RW	[7] dark current mode [6:4] BLK smooth speed [3:2] BLK Row select mode [1] dark current measure enable [0] offset enable
P0:0x28	Blk_limit_value	7	0x3f	RW	[7] NA [6:0] Blk value limit
P0:0x29	Col_gain_switch_not_smooth Global_offset	8	0x80	RW	[7] Col_gain_switch_not_smooth [6:0] global offset value
P0:0x2a	Current G1 offset	7	0x3c	RO	[7] NA [6:0] Current_G1_offset
P0:0x2b	Current R offset	7	0x3c	RO	[7] NA [6:0] Current R offset
P0:0x2c	Current B offset	7	0x3c	RO	[7] NA [6:0] Current B offset
P0:0x2d	Current G2 offset	7	0x3c	RO	[7] NA [6:0] Current G2 offset
P0:0x2e	Current G1 dark_current	7	0x3c	RO	[7] NA [6:0] Current G1 dark current
P0:0x2f	Current R dark_current	7	0x3c	RO	[7] NA [6:0] Current R dark current
P0:0x30	Current B dark_current	7	0x3c	RO	[7] NA [6:0] Current B dark current
P0:0x31	Current G2 dark_current	7	0x3c	RO	[7] NA [6:0] Current_G2_dark_current
P0:0x32	exp_rate_darkc	8	0x04	RW	Low 8 bits of 0.12; 4 means when exp=1024, dark current portion is 4
P0:0x33	offset_submode,offset_ratio G1	8	0x18	RW	[7:6] offset sub mode [5:0] offset ratio, 1.5 bits
P0:0x34	Offsetratio G2	6	0x18	RW	offset ratio, 1.5 bits
P0:0x35	offset_ratio R	6	0x18	RW	offset ratio, 1.5 bits
P0:0x36	offset_ratio B	6	0x18	RW	offset ratio, 1.5 bits
P0:0x37	darkc_submode dark_current_ratio G1	8	0x18	RW	[7:6] dark current sub mode [5:0] dark current ratio, 1.5 bits

P0:0x38	dark_current_ratio G2	6	0x18	RW	dark current ratio, 1.5 bits
P0:0x39	dark_current_ratio R	6	0x18	RW	dark current ratio, 1.5 bits
P0:0x3a	dark_current_ratio B	6	0x18	RW	dark current ratio, 1.5 bits
P0:0x3b	Manual_R_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3c	Manual_G1_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3d	Manual_G2_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3e	Manual_B_offset	6	0x00	RW	S5, aligned to lower 8 of 11 bits data
P0:0x3f	Reserved	4	0x02	RO	Reserved
P0:0x47	Global_offset_dark[9:8]	2	0x00	RW	Global_offset_dark[9:8]
P0:0x48	Global_offset_dark[7:0]	8	0x00	RW	Global_offset_dark[7:0]

Y Gamma

Address	Name	Width	Default Value	R/W	Description
P0:0x63	Y Gamma 0	8	0x00	RW	Knee0=0
P0:0x64	Y Gamma 1	8	0x10	RW	Knee1=8
P0:0x65	Y Gamma 2	8	0x1c	RW	Knee2=16
P0:0x66	Y Gamma 3	8	0x30	RW	Knee3=32
P0:0x67	Y Gamma 4	8	0x43	RW	Knee4=48
P0:0x68	Y Gamma 5	8	0x54	RW	Knee5=64
P0:0x69	Y Gamma 6	8	0x65	RW	Knee6=80
P0:0x6a	Y Gamma 7	8	0x75	RW	Knee7=96
P0:0x6b	Y Gamma 8	8	0x93	RW	Knee8=128
P0:0x6c	Y Gamma 9	8	0xb0	RW	Knee9=160
P0:0x6d	Y Gamma 10	8	0xcb	RW	Knee10=192
P0:0x6e	Y Gamma 11	8	0xe6	RW	Knee11=224
P0:0x6f	Y Gamma 12	8	0xff	RW	Knee12=256

PREGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x70	Global_gain	8	0x40	RW	Global gain
P0:0x71	Auto_pregain	8	0x40	RO	Controlled by AEC , can be manually controlled when disable AEC， float 4.4
P0:0x72	Auto_postgain	8	0x40	RO	Controlled by AEC , can be manually

					controlled when disable AEC, float 4.4
P0:0x73	Channel_gain_R	8	0x80	RW	G1 channel pre gain, float 1.7
P0:0x74	Channel_gain_G1	8	0x80	RW	R channel pre gain, float 1.7
P0:0x75	Channel_gain_G2	8	0x80	RW	B channel pre gain, float 1.7
P0:0x76	Channel_gain_B	8	0x80	RW	G2 channel pre gain, float 1.7
P0:0xeb	R_ratio	8	0x80	RW	R gain ratio, float 1.7
P0:0xec	G_ratio	8	0x80	RW	G gain ratio, float 1.7
P0:0xed	B_ratio	8	0x80	RW	B gain ratio, float 1.7
P0:0x77	AWB_R_gain	8	0x50	RO	2.6 bits, AWB red gain, controlled by AWB
P0:0x78	AWB_G_gain	8	0x40	RO	2.6 bits, AWB green gain, controlled by AWB
P0:0x79	AWB_B_gain	8	0x48	RO	2.6 bits, AWB blue gain, controlled by AWB

DNDD

Address	Name	Width	Default Value	R/W	Description
P0:0x7d	Reserved	6	0x1f	RO	Reserved
P0:0x7e	BFF_bilateral_b_base	6	0x1f	RW	[7:6] NA [5:0] BFF bilateral b base
P0:0x7f	1D DN mode	8	0x03	RW	[7] dn_1d_V enable [6] dn_1d_H enable [5] BFF_DN_1d_auto_b_enable [4:2] NA [1:0] bilateral c weight
P0:0x80	DN_mode_en	8	0x87	RW	[7] auto DD enable [6:5] DN select mode [4] NA [3] share mode [2] c_weight_adapt_mode [1] dn_lsc_mode [0] dn_b_mode
P0:0x81	DN_mode_ratio	8	0x22	RW	[7:6] bad ratio [5:4] C_weight_adaptive_ratio [3:2] dn_lsc_ratio [1:0] dn_b_mode_ratio

P0:0x82	DN_auto_disable DN_bilat_b_base	8	0x15	RW	[7] DN_auto_disable [6] NA [5:0] DN_bilat_b_base
P0:0x83	DN_C_weight	4	0x05	RW	[7:4] NA [3:0] DN_C_weight
P0:0x84	DD_dark_bright_TH	8	0xe5	RW	[7:4] dark threshold [3:0] bright threshold controlled by ASDE or user, should be set >=2
P0:0x85	DD_flat_TH	8	0x86	RW	DD flat THD
P0:0x86	DD_limit DD_ratio	6	0xf2	RW	[7:4] DD_limit [3:2] NA [1:0] DD_taio
P0:0x87	DN_b_in_dark_en DN_b_in_dark_inc_or_dec DD_mm_TH	8	0x8a	RW	[7] DN_b_in_dark_en [6] DN_b_in_dark_inc_or_dec [5:4] NA [3:0] DD_mm_TH
P0:0x88	DN_b_in_dark_th DN_b_in_dark_slope	8	0xff	RW	[7:4] DN_b_in_dark_th [3:0] DN_b_in_dark_slope
P0:0x89	Skin_edge_effect DNDD_skin_mode	8	0x10	RW	[7] NA [6] Skin edge effect [5:4] Effect skin ratio [3] NA [2] DNDD skin mode [1:0] DNDD skin ratio

INTPEE (Interpolation and Edge Enhancement)

Address	Name	Width	Default Value	R/W	Description
P0:0x90	EEINTP mode 1	8	0xac	RW	[7] edge mode1 [6] edge mode2 [5] edge2 direction mode [4] skin edge on [3] LP interpolation enable [2] LP edge enable [1:0] LP edge mode
P0:0x91	EEINTP mode 2	8	0x00	RW	[7] HP_mode1 [6] HP_mode2 [5] only 2 direction [4] USE_EE_mode_en [3] NA [2] NA

					[1:0] skin_ratio
P0:0x92	Direction TH1	6	0x05	RW	Lower Criteria for direction detection
P0:0x93	Direction TH2	6	0x3f	RW	Upper Criteria for direction detection
P0:0x94	Diff_HV_TI_TH Direction diff TH	8	0x05	RW	[7:4] Diff_HV_TI_TH [3:0] Direction diff TH
P0:0x95	Edge1 effect Edge2 effect	8	0x45	RW	[7:4] edge1 effect [3:0] edge2 effect Controlled by user or ASDE
P0:0x96	Edge_max Edge_TH	8	0x82	RW	[7:4] Edge_max [3:0] Edge_TH

ASDE (auto saturation de-noise and edge enhancement)

Address	Name	Width	Default Value	R/W	Description
P0:0x97	ASDE_TH1	8	0x20	RW	Reserved
P0:0x98	ASDE_low_luma_value_offset_slope	4	0x02	RW	ASDE low luma value offset slope
P0:0x99	Reserved	8	0x1e	RO	Reserved
P0:0x9a	ASDE Y offset limit	7	0x20	RW	ASDE Y offset limit
P0:0x9b	ASDE_THD2	8	0x60	RW	Reserved
P0:0x9c	ASDE_Y_offset_slope	4	0xa0	RW	[7:4] ASDE_Y_offset_slope [3:0] NA
P0:0x9d	Reserved	6	0x15	RO	Reserved
P0:0x9e	ASDE_DN_c_slope_high ASDE_DN_c_slope_low	8	0xaa	RW	[7:4] ASDE_DN_c_slope_high [3:0] ASDE_DN_c_slope_low
P0:0x9f	Reserved	4	0x08	RO	Reserved
P0:0xa0	ASDE_DD_bright_th_slope ASDE_DD_limit_slope	8	0x5f	RW	[7:4] ASDE_DD_bright_th_slope [3:0] ASDE_DD_limit_slope
P0:0xa1	Reserved	8	0x5f	RO	Reserved
P0:0xa2	ASDE_EE1_effect_slope_low ASDE_EE2_effect_slope_low	8	0x12	RW	[7:4] ASDE_EE1_effect_slope_low [3:0] ASDE_EE2_effect_slope_

					low
P0:0xa3	Reserved	8	0x45	RO	Reserved
P0:0xa4	ASDE_auto_saturation_dec_slope	8	0x10	RW	ASDE_auto_saturation_dec_slope
P0:0xa5	ASDE_auto_saturation_low_limit ASDE_sub_saturation_slope	8	0x31	RW	[7:4] ASDE_auto_saturation_low_limit [3:0] ASDE_sub_saturation_slope
P0:0xa6	ASDE_DD_mm_TH ASDE_DD_mm_th_slope	8	0xaa	RW	[7:4] ASDE_DD_mm_th. RO [3:0] ASDE_DD_mm_th_slope
P0:0xa7	ASDE_low_luma_value_DD_th	8	0x60	RW	ASDE_low_luma_value_DD_th
P0:0xa8	ASDE_LSC_gain_dec_slope	8	0x50	RW	ASDE_LSC_gain_dec_slope
P0:0xa9	Reserved	8	0xff	RO	Reserved
P0:0xaa	ASDE_THD3	8	0x60	RW	Reserved
P0:0xab	ASDE_EE1_effect_slope_high ASDE_EE2_effect_slope_high	8	0x12	RW	[7:4] ASDE_EE1_effect_slope_high [3:0] ASDE_EE2_effect_slope_high
P0:0xac	ASDE_DN_b_slope_high ASDE_DN_b_slope_low	8	0x66	RW	[7:4] ASDE_DN_b_slope_high [3:0] ASDE_DN_b_slope_low
P0:0xad	DN&EE ASDE mode	6	0x00	RW	[5] EE1_effect high luma mode [4] EE2_effect low luma mode [3] EE1_effect high luma mode [2] EE2_effect low luma mode [1] DN high luma mode [0] DN low luma mode

CC

Address	Name	Width	Default Value	R/W	Description
P0:0xb0	YCP_RGB2YC_mode	2	0x00	RW	[7:2] NA [1:0] YCP_RGB2YC_mode
P0:0xb1	CC Matrix C11	8	0x04	RW	R channel coefficient 1, S1.6
P0:0xb2	CC Matrix C12	8	0xfe	RW	R channel coefficient 2, S1.6
P0:0xb3	CC Matrix C13	8	0xfe	RW	R channel coefficient 3, S1.6
P0:0xb4	CC Matrix C21	8	0xfe	RW	G channel coefficient 1, S1.6
P0:0xb5	CC Matrix C22	8	0x04	RW	G channel coefficient 2, S1.6
P0:0xb6	CC Matrix C23	8	0xfe	RW	G channel coefficient 3, S1.6

RGB GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0xbf	Gamma_out0	8	0x10	RW	Each out value of knee i. Knee0=0
P0:0xc0	Gamma_out1	8	0x20	RW	Knee1=8
P0:0xc1	Gamma_out2	8	0x38	RW	Knee2=16
P0:0xc2	Gamma_out3	8	0x4e	RW	Knee3=24
P0:0xc3	Gamma_out4	8	0x63	RW	Knee4=32
P0:0xc4	Gamma_out5	8	0x76	RW	Knee5=40
P0:0xc5	Gamma_out6	8	0x87	RW	Knee6=48
P0:0xc6	Gamma_out7	8	0xa2	RW	Knee7=64
P0:0xc7	Gamma_out8	8	0xb8	RW	Knee8=80
P0:0xc8	Gamma_out9	8	0xca	RW	Knee9=96
P0:0xc9	Gamma_out10	8	0xd8	RW	Knee10=112
P0:0xca	Gamma_out11	8	0xe3	RW	Knee11=128
P0:0xcb	Gamma_out12	8	0xeb	RW	Knee12=144
P0:0xcc	Gamma_out13	8	0xf0	RW	Knee13 =160
P0:0xcd	Gamma_out14	8	0xf8	RW	Knee14 = 192
P0:0xce	Gamma_out15	8	0xfd	RW	Knee15 = 224
P0:0xcf	Gamma_out16	8	0xff	RW	Knee16 = 256

YCP

Address	Name	Width	Default Value	R/W	Description
P0:0xd0	Global saturation	8	0x40	RW	Global saturation, controlled by auto_saturation
P0:0xd1	saturation_Cb	8	0x40	RW	Cb saturation

					3.5bits, 0x20=1.0
P0:0xd2	saturation_Cr	8	0x40	RW	Cr saturation 3.5bits, 0x20=1.0
P0:0xd3	luma_contrast	8	0x40	RW	Luma_contrast, can be adjusted via contrast center 2.6bits, 0x40=1.0
P0:0xd4	Contrast center	8	0x80	RW	Contrast center value
P0:0xd5	Luma_offset	8	0x00	RW	Add offset on luma value. S7.
P0:0xd6	skin_Cb_center	8	0xe8	RW	Cb criteria for skin detection.
P0:0xd7	skin_Cr_center	8	0x20	RW	Cr criteria for skin detection.
P0:0xd8	Skin radius square	6	0x18	RW	Defines skin range
P0:0xd9	Skin brightness high Skin brightness low	8	0xe3	RW	[7:4] skin brightness high threshold [3:0] skin brightness low threshold
P0:0xda	Fixed_Cb	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cb value will be replace by this value to achieve special effect
P0:0xdb	Fixed_Cr	8	0x00	RW	S7, if fixed CbCr function is enabled, current image Cr value will be replace by this value to achieve special effect
P0:0xdc	Under_sun_mode	3	0x02	RW	[7:3] NA [2:0] under_sun_mode
P0:0xdd	Edge_dec_sa_en Edge_dec_sa_slope	7	0x38	RW	[7] NA [6:4] edge_dec_sa_en [3:0] edge_dec_sa_slope
P0:0xde	Sa_autogray mode Sa_autogray	6	0x36	RW	[7:6] NA [5:4] autogray mode [3:0] saturation autogray
P0:0xdf	Saturation_sub_strength	8	0x00	RO	Chroma offset in low light
P0:0xe0	Skin_bright_center	5	0x0f	RW	[7:5] NA [4:0] skin_bright_center
P0:0xe1	Y_delta	5	0x18	RW	[7:5] NA [4:0] Y_delta
P0:0xe2	Skin_RR_halo_radius	6	0x20	RW	[7:6] NA [5:0] skin_RR_halo_radius
P0:0xe3	Exp_under_sun_th	8	0x32	RW	Exp_under_sun_th
P0:0xe4	Asde_autogray_en	8	0x08	RW	[7] asde autogray enable [6:4] NA [3:0] Autogray slope
P0:0xe5	Autogray THD	8	0x40	RW	Autogray THD
P0:0xe6	Reserved	5	0x0c	RO	Reserved
P0:0xee	Auto cc mode	8	0x80	RW	auto CC mode
P0:0xef	Auto cc THD	8	0x40	RW	auto CC THD

ABB

Address	Name	Width	Default Value	R/W	Description
P0:0xe7	ABB_mode	6	0x1a	RW	[7:6] NA [5] ABB enable [4] ABB smooth enable [3:0] ABB diff_max
P0:0xe8	ABB_speed	7	0x40	RW	[7] NA [6:4] ABB n min [3] NA [2:0] ABB speed
P0:0xe9	ABB_dark_th	6	0x20	RW	[7:6] NA [5:0] ABB dark THD
P0:0xea	ABB_keep_th	8	0xff	RW	ABB keep THD

Measure Window

Address	Name	Width	Default Value	R/W	Description
P1:0x06	big_win_x0	8	0x08	RW	Window setting for AEC & AWB
P1:0x07	big_win_y0	8	0x06	RW	
P1:0x08	big_win_x1	8	0xa8	RW	
P1:0x09	big_win_y1	8	0xf4	RW	
P1:0x0a	small_win_width1	8	0x32	RW	Col1 width, x4
P1:0x0b	small_win_height1	8	0x28	RW	Row1 height, x4
P1:0x0c	small_win_width2	8	0x64	RW	Col2 width
P1:0x0d	small_win_height2	8	0x50	RW	Row2 height

AEC

Address	Name	Width	Default Value	R/W	Description
P1:0x10	AEC_mode1	8	0x18	RW	[7] adapt weight mode [6] Reserved [5:4] exp mode [5] one step mode [4] fix gain exp mode [3] measure point [2] gain mode [1] AEC adjust mode [0] skip mode
P1:0x11	AEC_mode2	8	0xa1	RW	[7] fix target mode

					[6:4] AEC take action every N frame [3:2] close frame number to eliminate bad frame [1] change exp gain mode [0] dead zone mode
P1:0x12	AEC_mode3	8	0x20	RW	[7] map measure point [6:4] center weight mode [3:2] skin weight mode [1:0] NA
P1:0x13	AEC_target_Y_start	8	0x80	RW	expected luminance value
P1:0x14	Y_average	8	0x80	RO	Current frame luma average
P1:0x15	AEC_high_range	8	0xf2	RW	count limit for high luminance pixels
P1:0x16	AEC_select_mode AEC_low_range	8	0x98	RW	[7:6] high [5:4] low [3:0] count limit for low luminance pixels x4
P1:0x17	AEC_ignore	8	0x18	RW	[7] ignore mode enable [3:0] Reserved
P1:0x18	AEC_luma_div	8	0x03	RW	[7:3] NA [2:0] luma value divider
P1:0x1a	AEC_slow_margin AEC_slow_speed	7	0x91	RW	[7:4] AEC slow margin, X4 [3] NA [2:0] AEC slow speed
P1:0x1b	AEC_fast_margin AEC_fast_speed	7	0x96	RW	[7:4] AEC fast margin, X4 [3] NA [2:0] AEC fast speed
P1:0x1c	AEC_exp_change_ gain_ratio	8	0x96	RW	Gain change criteria, float 1.7, default use 1.2x
P1:0x1d	AEC_step2_sunlight	8	0x01	RW	AEC_step2_sunlight
P1:0x1e	AEC_I_frames AEC_D_ratio	6	0x33	RW	[7:6] NA [5:4] mode for Y difference selection [3:0] differential coefficient in AEC control algorithm
P1:0x1f	AEC_I_stop_L _margin	7	0x07	RW	[7] NA [6:0] x2, Will be used as AEC convergence margin
P1:0x20	AEC_I_stop_margin AEC_I_ratio	8	0x41	RW	[7:4] AEC adjust stop margin [3:0] integration coefficient
P1:0x21	AEC_max_pose_	8	0xc0	RW	The max post-gain AEC can

	dg_gain				output.
P1:0x22	AEC_max_pre_dg_gain	8	0x60	RW	The max pre-gain AEC can output.
P1:0x23	AEC_max_dg_gain	8	0x20	RW	Max Dgain for new exp mode
P1:0x24	AEC max exp index	8	0x22	RW	[7:3] Reserved [2:0] AEC max exp index
P1:0x25	Reserved	8	0x00	RW	Reserved
P1:0x26	Reserved	8	0x40	RW	Reserved
P1:0x27	Reserved	8	0x20	RW	Reserved
P1:0x28	Reserved	4	0x00	RW	Reserved
P1:0x29	AEC_anti_flicker_step[11:8]	4	0x00	RW	Anti-flicker step[11:8]
P1:0x2a	AEC_anti_flicker_step[7:0]	8	0x96	RW	Anti-flicker step[7:0]
P1:0x2b	AEC_exp_level_0[11:8]	4	0x02	RW	Exposure level 0
P1:0x2c	AEC_exp_level_0[7:0]	8	0x58	RW	
P1:0x2d	AEC_exp_level_1[11:8]	4	0x03	RW	Exposure level 1
P1:0x2e	AEC_exp_level_1[7:0]	8	0x84	RW	
P1:0x2f	AEC_exp_level_2[11:8]	4	0x07	RW	Exposure level 2
P1:0x30	AEC_exp_level_2[7:0]	8	0x08	RW	
P1:0x31	AEC_exp_level_3[11:8]	4	0x0d	RW	Exposure level 3
P1:0x32	AEC_exp_level_3[7:0]	8	0x7a	RW	
P1:0x33	AEC_max_exp_level AEC_exp_min_l[11:8]	6	0x20	RW	[7:6] NA [5:4] Max level setting [3:0] exp_min[11:8]
P1:0x34	AEC_exp_min_l[7:0]	8	0x04	RW	exp_min[7:0]
P1:0x35	AEC_ratio_low_thd	8	0x20	RW	AEC ratio low threshold
P1:0x36	AEC_ratio_high_thd	8	0x60	RW	AEC ratio high threshold
P1:0x37	AEC_weight_min_limit	8	0x04	RW	AEC weight min limit
P1:0x38	AEC_weight_max_limit	8	0xf0	RW	AEC weight max limit
P1:0x39	AEC_more_gain_div0	7	0x4f	RW	[7] NA [6:0] AEC more gain div0

P1:0x3c	Reserved	8	0x50	RW	Reserved
P1:0x3d	Reserved	8	0x40	RW	Reserved
P1:0x3e	Reserved	8	0x30	RW	Reserved
P1:0x3f	Reserved	8	0x80	RO	Reserved
P1:0x40	Reserved	8	0x80	RO	Reserved
P1:0x41	Reserved	8	0x80	RO	Reserved
P1:0x42	Reserved	8	0x80	RO	Reserved
P1:0x43	Reserved	8	0x80	RO	Reserved
P1:0x44	Reserved	8	0x80	RO	Reserved
P1:0x8f	Reserved	8	0x00	RO	Reserved

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x4c	Reserved	8	0x00	RW	Reserved
P1:0x4d	Reserved	8	0x00	RW	Reserved
P1:0x4e	Reserved	8	0x00	RO	Reserved
P1:0x4f	Reserved	1	0x00	RW	Reserved
P1:0x50	AWB_PRE_mode	8	0x00	RW	[7] PRE_enable [6:0] Reserved
P1:0x51	AWB_PRE_THD_min[7:0]	8	0x80	RW	Dominate luma THD
P1:0x52	AWB_PRE_THD_min[15:8]	8	0x01	RW	
P1:0x53	AWB_PRE_THD_min_MIX[7:0]	8	0x80	RW	mix luma number THD
P1:0x54	AWB_PRE_THD_min_MIX[15:8]	8	0x0f	RW	
P1:0x55	AWB_PRE_pixel_select_mode	8	0x00	RW	pre AWB debug pixel select
P1:0x56	AWB_tone_mode	8	0x00	RW	AWB tone mode
P1:0x57	AWB_PRE_adjust_speed	8	0x20	RW	Adjust speed
P1:0x58	AWB_num_sel	8	0x00	RW	[7:6] NA [5:4] AWB_C_num_sel [3:2] Reserved [1:0] AWB_D_num_sel
P1:0x59	AWB_PRE_RGB_low	8	0x01	RW	RGB pixel low THD
P1:0x5a	AWB_PRE_RGB_high	8	0xf0	RW	RGB pixel high THD

P1:0x5b	AWB_gain_delta	8	0x0f	RW	mix base gain and adaptive gain limit
P1:0x5c~P1:0x63 Reserved					
P1:0x65	Reserved	8	0x40	RO	Reserved
P1:0x66	Reserved	8	0x40	RO	Reserved
P1:0x67	Reserved	8	0x40	RO	Reserved
P1:0x68	Reserved	6	0x00	RO	Reserved
P1:0x69	Reserved	8	0x00	RO	Reserved
P1:0x6a	Reserved	8	0x00	RO	Reserved
P1:0x6b	Reserved	4	0x05	RO	Reserved
P1:0x6c	Reserved	8	0x00	RO	Reserved
P1:0x6d	Reserved	8	0x00	RO	Reserved
P1:0x6e	Reserved	8	0x05	RO	Reserved
P1:0x6f	Reserved	8	0x00	RO	Reserved
P1:0x70	AWB_RGB_high	8	0xf5	RW	AWB high range
P1:0x71	AWB_RGB_low	8	0x0a	RW	AWB low range
P1:0x72	AWB Y2C	8	0x18	RW	AWB Y to C difference
P1:0x73	AWB_C_inter	8	0x20	RW	AWB C inter
P1:0x74	AWB_C_max	8	0x20	RW	AWB C max
P1:0x75	AWB_out_mode	8	0x00	RW	Reserved
P1:0x76	AWB_move_mode	8	0x8f	RW	[7] move mode [6:0] move THD
P1:0x77	AWB_uplow_luma_ value	8	0xe0	RW	AWB luma value THD
P1:0x78	AWB_number_limit	8	0xa0	RW	AWB number limit
P1:0x79	AWB_gain_mix_ mode AWB_sel_point AWB_skip_mode	8	0x00	RW	[7:4] AWB_gain_mix_mode [3] NA [2] AWB_sel_point [1:0] AWB_skip_mode
P1:0x7a	AWB_light_gain_ range	8	0x30	RW	dark mode luma level THD
P1:0x7b	show_and_mode	8	0x34	RW	[7:6] AWB show select mode [5] skin_mode [4:2] NA [1] dark_mode [0] NA
P1:0x7c	adjust_speed adjust_margin	8	0x42	RW	[7] NA [6:4] AWB gain adjust speed [3:0] if averages of R/G/B's difference is smaller than margin, it means AWB is OK,

					and AWB will stop.
P1:0x7d	AWB_every_N	2	0x20	RW	[7:6] NA [5:4] AWB_every_N [3:0] NA
P1:0x80	AWB_R_gain_limit	8	0x70	RW	channel gain limit for R.
P1:0x81	AWB_G_gain_limit	8	0x58	RW	channel gain limit for G.
P1:0x82	AWB_B_gain_limit	8	0x78	RW	channel gain limit for B.
P1:0x83	AWB R gain limit1	8	0x50	RW	AWB R gain limit1
P1:0x84	AWB G gain limit1	8	0x58	RW	AWB G gain limit1
P1:0x85	AWB B gain limit1	8	0x46	RW	AWB B gain limit1
P1:0x86	AWB R gain limit2	8	0x40	RW	AWB R gain limit2
P1:0x87	AWB G gain limit2	8	0x40	RW	AWB G gain limit2
P1:0x88	AWB B gain limit2	8	0x40	RW	AWB B gain limit2
P1:0x89	Reserved	8	0x40	RO	Reserved
P1:0x8a	Reserved	8	0x40	RO	Reserved
P1:0x8b	Reserved	8	0x40	RO	Reserved

ABS

Address	Name	Width	Default Value	R/W	Description
P1:0x9a	ABS_mode	7	0x03	RW	[7:4] ABS range [3] NA [2:0] ABS skip frames
P1:0x9b	ABS_stop_ margin	4	0x02	RW	[7:4] NA [3:0] margin for ABS to stop adjustment
P1:0x9c	Y_S_ compensate ABS_ manual_K	8	0x01	RW	[7:4] Y stretch compensate [3:0] manual ABS slope adjustment, default 0
P1:0x9d	Y_stretch_ limit	8	0x20	RW	[7:0] Y stretch limit
P1:0x9e	Reserved	8	0xc0	RO	Reserved
P1:0x9f	Reserved	8	0x40	RO	Reserved

LSC

Address	Name	Width	Default Value	R/W	Description
P1:0xa1	LSC_row_ center	7	0x3c	RW	LSC_row_center, the real value is this setting X4.

P1:0xa2	LSC_col_ center	8	0x50	RW	LSC_col_center, the real value is this setting X4.
P1:0xa4	LSC_para_ sign1	6	0x00	RW	[6] LSC_Q1_red_b1_signed [5] LSC_Q1_green_b1_signed [4] LSC_Q1_blue_b1_signed [2] LSC_Q2_red_b1_signed [1] LSC_Q2_green_b1_signed [0] LSC_Q2_blue_b1_signed
P1:0xa5	LSC_para_ sign2	6	0x00	RW	[6] LSC_Q3_red_b1_signed [5] LSC_Q3_green_b1_signed [4] LSC_Q3_blue_b1_signed [2] LSC_Q4_red_b1_signed [1] LSC_Q4_green_b1_signed [0] LSC_Q4_blue_b1_signed
P1:0xa6	LSC_para_ sign3	6	0x00	RW	[6] LSC_right_red_b4_signed [5] LSC_right_green_b4_signed [4] LSC_right_blue_b4_signed [2] LSC_left_red_b4_signed [1] LSC_left_green_b4_signed [0] LSC_left_blue_b4_signed
P1:0xa7	LSC_para_ sign4	6	0x00	RW	[6] LSC_top_red_b4_signed [5] LSC_top_green_b4_signed [4] LSC_top_blue_b4_signed [2] LSC_bottom_red_b4_signed [1] LSC_bottom_green_b4_signed [0] LSC_bottom_blue_b4_signed
P1:0xa8	LSC_Q1_red_ b1	8	0x20	RW	LSC_Q1_red_b1
P1:0xa9	LSC_Q1_ green_b1	8	0x20	RW	LSC_Q1_green_b1
P1:0xaa	LSC_Q1_blue_ b1	8	0x20	RW	LSC_Q1_blue_b1
P1:0xab	LSC_Q2_red_ b1	8	0x20	RW	LSC_Q2_red_b1
P1:0xac	LSC_Q2_ green_b1	8	0x20	RW	LSC_Q2_green_b1
P1:0xad	LSC_Q2_blue_ b1	8	0x20	RW	LSC_Q2_blue_b1
P1:0xae	LSC_Q3_red_ b1	8	0x20	RW	LSC_Q3_red_b1
P1:0xaf	LSC_Q3_green _b1	8	0x20	RW	LSC_Q3_green_b1

P1:0xb0	LSC_Q3_blue_b1	8	0x20	RW	LSC_Q3_blue_b1
P1:0xb1	LSC_Q4_red_b1	8	0x20	RW	LSC_Q4_red_b1
P1:0xb2	LSC_Q4_green_b1	8	0x20	RW	LSC_Q4_green_b1
P1:0xb3	LSC_Q4_blue_b1	8	0x20	RW	LSC_Q4_blue_b1
P1:0xb4	LSC_right_red_b2	8	0x20	RW	LSC_right_red_b2
P1:0xb5	LSC_right_green_b2	8	0x20	RW	LSC_right_green_b2
P1:0xb6	LSC_right_blue_b2	8	0x20	RW	LSC_right_blue_b2
P1:0xb7	LSC_right_red_b4	8	0x20	RW	LSC_right_red_b4
P1:0xb8	LSC_right_green_b4	8	0x20	RW	LSC_right_green_b4
P1:0xb9	LSC_right_blue_b4	8	0x20	RW	LSC_right_blue_b4
P1:0xba	LSC_left_red_b2	8	0x20	RW	LSC_left_red_b2
P1:0xbb	LSC_left_green_b2	8	0x20	RW	LSC_left_green_b2
P1:0xbc	LSC_left_blue_b2	8	0x20	RW	LSC_left_blue_b2
P1:0xbd	LSC_left_red_b4	8	0x20	RW	LSC_left_red_b4
P1:0xbe	LSC_left_green_b4	8	0x20	RW	LSC_left_green_b4
P1:0xbf	LSC_left_blue_b4	8	0x20	RW	LSC_left_blue_b4
P1:0xc0	LSC_top_red_b2	8	0x20	RW	LSC_top_red_b2
P1:0xc1	LSC_top_green_b2	8	0x20	RW	LSC_top_green_b2
P1:0xc2	LSC_top_blue_b2	8	0x20	RW	LSC_top_blue_b2
P1:0xc3	LSC_top_red_b4	8	0x20	RW	LSC_top_red_b4
P1:0xc4	LSC_top_green_b4	8	0x20	RW	LSC_top_green_b4

P1:0xc5	LSC_top_blue_b4	8	0x20	RW	LSC_top_blue_b4
P1:0xc6	LSC_bottom_red_b2	8	0x20	RW	LSC_bottom_red_b2
P1:0xc7	LSC_bottom_green_b2	8	0x20	RW	LSC_bottom_green_b2
P1:0xc8	LSC_bottom_blue_b2	8	0x20	RW	LSC_bottom_blue_b2
P1:0xc9	LSC_bottom_red_b4	8	0x20	RW	LSC_bottom_red_b4
P1:0xca	LSC_bottom_green_b4	8	0x20	RW	LSC_bottom_green_b4
P1:0xcb	LSC_bottom_blue_b4	8	0x20	RW	LSC_bottom_blue_b4